ADM6999G/GX

8 port 10/100 Mb/s + Gigabit Single Chip Ethernet Switch Controller

Communications

Never stop thinking.

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Previous Version:

Page/Date	Subjects (major changes since last revision)
2002-08	Rev. 0.1: First ADMtek version
2002-09	Rev. 1.0: Remove Preliminary word
2002-12	Rev. 1.1: Modify error word; Add GMII timing
2003-04	Rev. 1.2: Modify GMII receive setup time and hold time. GRXER change to GND or NC. Modify MII RXCLK & TXCLK timing requirement.
2003-05	Rev. 1.3: Modify RTX to 1K 1% at A2 version chip
2005-05	Rev. 1.31: Changed to the new Infineon format
2005-11-25	Minor change. Included Green package information

Trademarks

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1 Introduction

1.1 General Description

The ADM6999G/GX is a high performance, low cost, and highly integration (Controller, PHY and Memory) eight-port 10/100 Mbps TX/FX plus one 10/100/1000 GMII port Ethernet switch controller with all ports supporting 10/100 Mbps Full/Half duplex and Gigabit port support Full Duplex switch function. The ADM6999G/GX is intended for applications to stand alone the bridge for low cost SOHO market such as 8+1G. The ADM6999GX is the environmentally friendly “green” package version.

ADM6999G/GX provides most advanced functions such as: **802.1p (Q.O.S.), 802.1q (VLAN), Port MAC Address Locking, Management, Port Status, TP Auto-MDIX, 25M Crystal & Extra ninth Port (GMII)** functions to meet the customer’s requests on Switch demand.

The built-in 768K SRAM used for the packet buffer and address learning table is divided into 512 bytes/block to achieve the optimized memory utilization through complicated link list on packets with various lengths.

ADM6999G/GX also supports priority features by Port-Base, VLAN and IP TOS field checking. Users can easily set a different priority mode in individual port, through a small low-cost micro controller to initialize or on-the-fly to configure. Each output port supports two queues in the way of fixed N: 1 fairness queuing to fit the bandwidth demand on various types of packet such as Voice, Video and data. 802.1Q, Tag/Untag, and up to 32 groups of VLAN are also supported. ADM6999G/GX learns user to define 4 or 5 bits of VLAN ID.

An intelligent address recognition algorithm makes ADM6999G/GX to recognize up to 2048 different MAC addresses and enables filtering and forwarding at full wire speed.

Port MAC address Locking function is also supported by ADM6999G/GX to use on Building Internet access to prevent multiple users share one port traffic.

1.2 Features

Main features:

- Supports eight 10M/100M auto-detect Half/Full duplex switch ports with TX/FX interfaces and one GMII/MII port.
- Built-in 12Kx64 SRAM
- Supports 2048 MAC addresses table
- Supports two queue for Qos
- Supports priority features by Port-Based, 802.1p VLAN & IP TOS of packets
- Supports Store & Forward architecture and performs forwarding and filtering at non-blocking full wire speed
- Supports buffer allocation with 512 bytes per block
- Supports Aging function Enable/Disable
- Supports serial Single/Dual color mode with Power On auto diagnostic.
- Supports 802.3x Flow Control pause packet for Full Duplex in case buffer is full
- Supports Back Pressure function for Half Duplex operation in case buffer is full
- Supports packet length up to 1522 bytes
- Broadcast Storming Filter function
- Supports 802.1Q VLAN. Up to 16/32 VLAN groups are implemented by the user to define four/five bits of VLAN ID
- Supports MAC-clone feature
- Supports TP interface **Auto MDIX** function for auto TX/RX swap by strapping-pin
- Easy Management 32bits smart counter for per port RX/TX byte/packet count, error count and collision count
- Supports PHY status output for management system
- 25M Crystal only for the whole system. Output 10M/25M/50M for different interface
- 128 QFP package with 0.18um technology. 1.8 V/3.3 V power supply

1.3 Applications

ADM6999G/GX in 128-pin PQFP:

- Standalone SOHO 8+1 Gigabit Switch as start-kit
- Gigabit up link module, etc..

2 Input and Output Signals

This chapter describes Pin Diagram and Pin Descriptions.

2.1 Pin Diagram

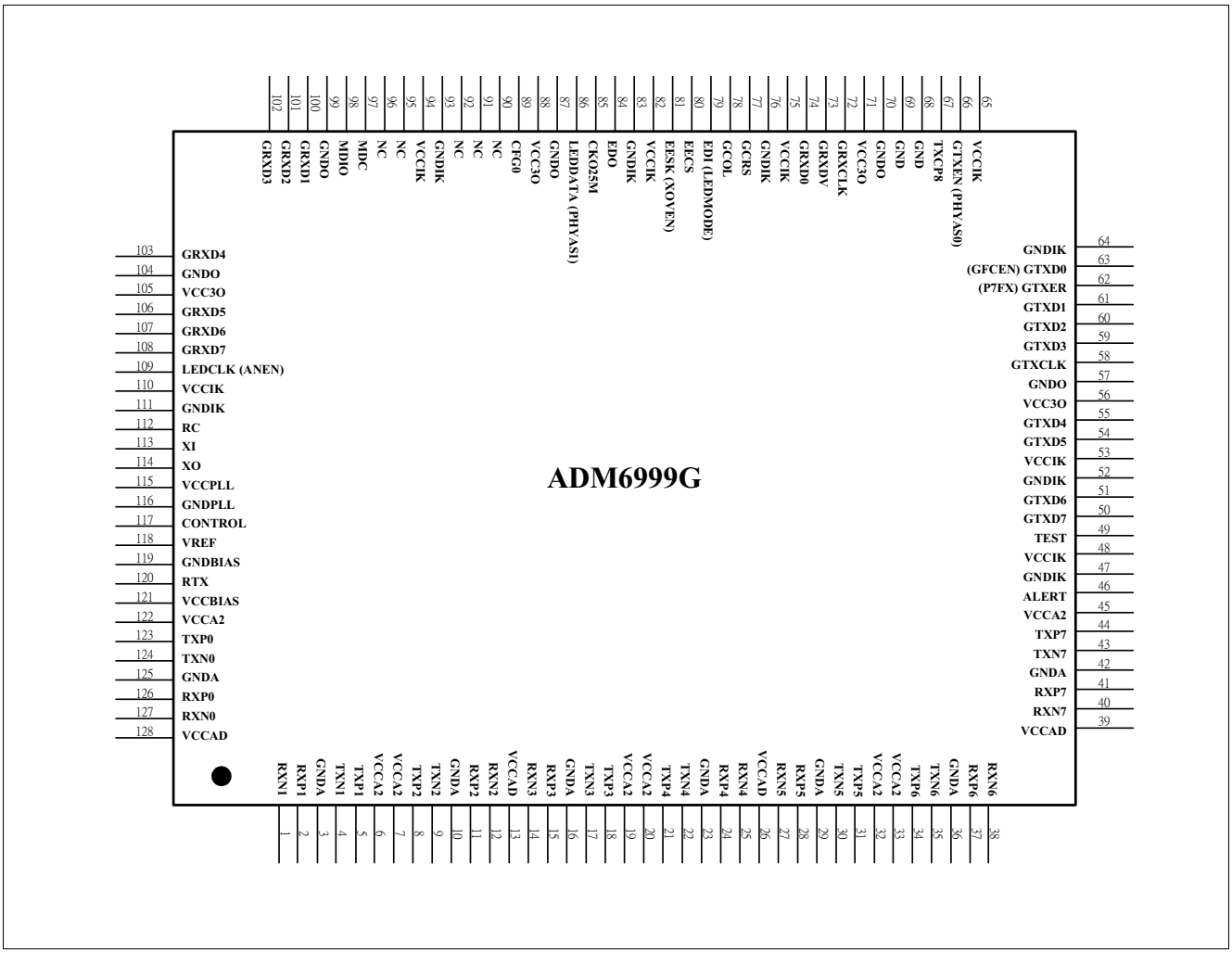


Figure 1 8 TP/FX PORT + 1 GMII PORT 128 Pin Diagram

2.2 Pin Type and Buffer Type Abbreviations

Standardized abbreviations:

Table 1 Abbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or Output. Analog levels.
PWR	Power
GND	Ground
MCL	Must be connected to Low (JEDEC Standard)
MCH	Must be connected to High (JEDEC Standard)
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 2 Abbreviations for Buffer Type

Abbreviations	Description
Z	High impedance
PU1	Pull up, 10 kΩ
PD1	Pull down, 10 kΩ
PD2	Pull down, 20 kΩ
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
OC	Open Collector
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).
OD/PP	Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute.
ST	Schmitt-Trigger characteristics
TTL	TTL characteristics

2.3 Pin Descriptions

Table 3 ADM6999G/GX-128 PINS(8 TP + GPSI/RMII)[1)2)]

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Twisted Pair Interface				
126	RXP0	AI/O		**Twisted Pair Receive Input Positive**
2	RXP1			
11	RXP2			
15	RXP3			
24	RXP4			
28	RXP5			
37	RXP6			
41	RXP7			
127	RXN0	AI/O		**Twisted Pair Receive Input Negative**
1	RXN1			
12	RXN2			
14	RXN3			
25	RXN4			
27	RXN5			
38	RXN6			
40	RXN7			
123	TXP0	AI/O		**Twisted Pair Transmit Output Positive**
5	TXP1			
8	TXP2			
18	TXP3			
21	TXP4			
31	TXP5			
34	TXP6			
44	TXP7			
124	TXN0	AI/O		**Twisted Pair Transmit Output Negative**
4	TXN1			
9	TXN2			
17	TXN3			
22	TXN4			
30	TXN5			
35	TXN6			
43	TXN7			
Ninth Port (GMII) Interfaces				

Table 3 ADM6999G/GX-128 PINS(8 TP + GPSI/RMII)[1)2)] (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
63	GTXD0	I/O	8mA, PU	**Giga Port transmit data 0** Acts as GMII transmit data TXD0 synchronous to the rising edge of TXCLK
	GFCEN	I/O	8mA, PU	**Setting GFCEN: Global Flow Control Enable.** At power-on-reset, latched as Flow control setting 0_B , Disable flow-control 1_B , Enable flow-control (default)
61	GTXD1	O	8mA	**Giga Port Transmit Data bit 1~7** Synchronous to the rising edge of GTXCLK
60	GTXD2			
59	GTXD3			
55	GTXD4			
54	GTXD5			
51	GTXD6			
50	GTXD7			
62	P7FX	I/O	8mA, PD	**Setting Port7 FX/TX Mode select** Internal pull down. 0_B , Port7 as TX port 1_B , Port7 as FX port
	GTXER	I/O	8mA, PD	**Giga Port Transmit Error**
66	PHYAS0	I/O	8mA, PD	**Setting PHYAS0: Chip physical address0 for multiple chip application on EEPROM access.** Internal pull down Power on reset value PHYAS0 combines with PHYAS1(LEDDATA). PHYAD Gigabit PHY Address 00 08_H Master Master: ADM6999G/GX will read 93C46 EEPROM first Bank.(00_H~27_H). If there is no EEPROM then user must use 93C66 timing to write chip's register. If user put 93C46 with correct Signature then user writes chip register by 93C46 timing. If user put 93C66 then data put in Bank0. User can write chip register by 93C66 timing. User must assert one SK cycle when CS is at idle stage and chip internal registers are being writing.
	GTXEN	I/O	8mA, PD	**Giga Port Transmit Enable.**

Table 3 ADM6999G/GX-128 PINS(8 TP + GPSI/RMII)[1)2)] (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
74	GRXD0	I	PD	**Giga Port receive data 0~7** Synchronous to the rising edge of RXCLK
100	GRXD1			
101	GRXD2			
102	GRXD3			
103	GRXD4			
106	GRXD5			
107	GRXD6			
108	GRXD7			
73	GRXDV	I	PD	**Giga Port receive data valid** Internal pull down
68	GND	I	PD	**GND or NC at normal application**
78	GCOL	I	PD	**MII Port Collision input** Internal pull down
77	GCRS	I	PD	**Giga Port Carrier Sense** Internal pull down
58	GTXCLK	O	16mA	**Gigabit Port 125 MHz clock Output**
72	GRXCLK	I		**Giga Port Receive Clock Input**
67	TXCP8	I		**MII Port Transmit clock Input**
LED Interface				
86	LEDDATA			**Serial LED Data**
	PHYAS1			**Setting PHYAS1: Chip physical address1 for multiple chip application on EEPROM access.** Internal pull down. See pin 66.
109	LEDCLK			**Serial LED Clock**
	ANEN			**Setting ANEN: On power-on-reset, latched as Auto Negotiation capability for all ports.** 0_B , Disable Auto Negotiation 1_B , Enable Auto Negotiation (defaulted by pulled up internally)
EEPROM/Management Interface				
84	EEDO	I	TTL, PU	**EEPROM Data Output** Serial data input from EEPROM. This pin is internally pull-up.
80	EECS	O	4mA, PD	**EEPROM Chip Select** This pin is an active high chip enable for EEPROM. When RC is low, it will be Tristate. This pin is internally pull-down.

Table 3 ADM6999G/GX-128 PINS(8 TP + GPSI/RMII)[1)2)] (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
81	EECK	I/O	4mA, PD	**Serial Clock** This pin is clock source for EEPROM.
	XOVEN	I/O	4mA, PD	**Setting XOVEN: This pin is internally pull-down.** On power-on-reset, latched as P7~0 Auto MDIX enable or not. Suggests externally pull up to enable Auto MDIX for all ports. 0_B , Disable MDIX (defaulted) 1_B , Enable MDIX
79	EEDI	O	4mA, PD	**EEPROM Serial Data Input** This pin is output for serial data transfer.
	LEDMODE	O	4mA, PD	**Setting LEDMODE** This pin is internally pull-down. On power-on-reset, latched as Dual Color mode or not. 0_B , Single Color LED 1_B , Dual Color LED
98	MDIO	I/O	8mA	**Management Data** This pin is in-out to PHY. When RC is low, this pin will be tri-state.
97	MDC	O	8mA	**Management Data Clock** This pin output 1 MHz clock to drive PHY and access corresponding speed and duplex data through MDIO.
Misc.				
85	CKO25M	O	8mA	**25M Clock Output For GMII port**
117	Control	O		**FET Control Signal** The pin is used to control FET for 3.3 V to 1.8 V regulator. Add 0.01 µf capacitor to GND.
120	RTX	A		**TX Resistor** Add 1.1K %1(A1), 1K %1 (A2) resister to GND.
118	VREF	A		**Analog Reference Voltage**
112	RC	I	ST	**RC Input for Power On reset** Reset input pin
113	XI	AI		**25M Crystal Input** 25M Crystal Input. Variation is limited to +/- 50ppm.
114	XO	AO		**25M Crystal Output** When connected to oscillator, this pin should be left unconnected.
49	TEST	I	TTL	**TEST Value** At normal application connects to GND.
Chip Configuration				
89	CFG0	I	TTL, PU	**Must Connected to GND**
46	ALERT	O		**Alert LED Display** This pin will show the status of power-on-diagnostic and broadcast traffic.

Table 3 ADM6999G/GX-128 PINS(8 TP + GPSI/RMII)[1)2)] (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Power/Ground				
3, 10, 16, 23, 29, 36, 42, 125	GNDA	I		**Ground Used by AD Block**
6, 7, 19, 20, 32, 33, 45, 122	VCCA2	I		**1.8 V, Power Used by TX Line Driver**
13, 26, 39, 128	VCCAD	I		**3.3 V, Power Used by AD Block**
119	GNDBIAS	I		**Ground Used by Bias Block**
121	VCCBIAS	I		**3.3 V, Power Used by Bias Block**
116	GNDPLL	I		**Ground used by PLL**
115	VCCPLL	I		**1.8 V, Power used by PLL**
47, 52, 64, 76, 83, 93, 111	GNDIK	I		**Ground Used by Digital Core**
48, 53, 65, 75, 82, 94, 110	VCCIK	I		**1.8 V, Power Used by Digital Core**
57, 70, 87, 99, 104	GNDO	I		**Ground Used by Digital Pad**
56, 71, 88, 105	VCC3O	I		**3.3 V, Power Used by Digital Pad**
69	GND	I	TTL	**Scan Enable** This pin will be used as the scan enable input for testing. Connects to GND at normal application.
NC pins				
90, 91, 92, 95, 96	NC			**No Connect**

1) Do not swap TP port +- signal. It may cause link fail when link partner does not support Auto Polarity function.

2) I: Input, O: Output, I/O: Bi-directional, OD: Open drain, SCHE: Schmitt-Trigger, PD: internal pull-down, PU: internal pull-up

3 Descriptions

This chapter provides Functional Description, 10/100M PHY Block Description, Memory Block Description, Switch Functional Description, EEPROM Content and EEPROM Access Description.

3.1 Functional Description

The ADM6999G/GX integrates eight 100Base-X physical sub-layer (PHY), 100Base-TX physical medium dependent (PMD) transceivers, eight complete 10Base-T modules, 8 port 100/10 switch controller, and one 10/100/1000 MAC and memory into a single chip for both 10Mbits/s, 100Mbits/s, 1000Mbits/s Ethernet switch operations. It also supports 100Base-FX operation through external fiber-optic transceivers. The device is capable of operating in either Full Duplex mode, Half-Duplex mode in 10Mbits/s and 100Mbits/s, or Full duplex only at 1000Mbits/s operation. Operational modes can be selected by hardware configuration pins, software settings of management registers, or determined by the on-chip auto negotiation logic.

The ADM6999G/GX consists of three major blocks:

- 10/100M PHY Block
- Switch Controller Block
- Built-in 12Kx64 SSRAM

3.2 10/100M PHY Block Description

The 100Base-X section of the device implements the following functional blocks:

- 100Base-X physical coding sub-layer (PCS)
- 100Base-X physical medium attachment (PMA)
- Twisted-pair transceiver (PMD)

The 100Base-X and 10Base-T sections share the following functional blocks:

- Clock synthesizer module
- MII Registers
- IEEE 802.3u auto negotiation

3.2.1 100Base-X Module

The ADM6999G/GX implements 100Base-X compliant PCS, PMA and 100Base-TX compliant TP-PMD as illustrated in **Figure 2**. Bypass options for each of the major functional blocks within the 100Base-X PCS provide flexibility for various applications. 100Mbits/s PHY loop back is included for the diagnostic purpose.

3.2.2 100Base-X Receiver

The 100Base-X receiver consists of functional blocks required to recover and condition the 125Mbits/s received data stream. The ADM6999G/GX implements the 100Base-X received state machine diagram as given in ANSI/IEEE Standard 802.3u, Clause 24. The 125Mbits/s received data stream may originate from the on-chip twisted-pair transceiver in a 100Base-TX application. Alternatively, the received data stream may be generated by an external optical receiver as in a 100Base-FX application.

The receiver block consists of the following functional sub-blocks:

- A/D Converter
- Adaptive Equalizer and timing recovery module
- NRZI/NRZ and serial/parallel decoder
- De-scrambler
- Symbol alignment block
- Symbol Decoder
- Collision Detect Block
- Carrier sense Block

- Stream decoder block

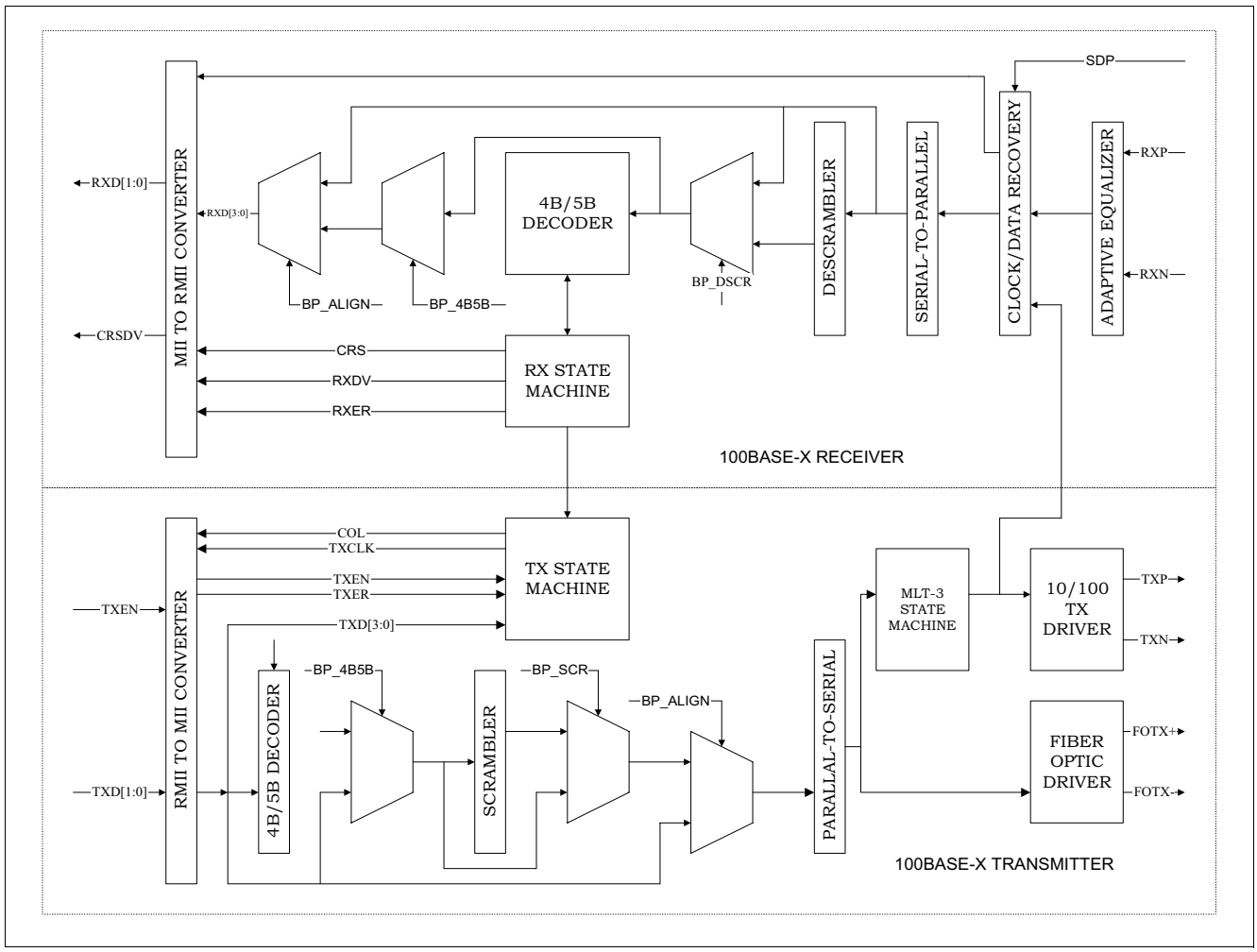


Figure 2 100Base-X Module

3.2.2.1 A/D Converter

High performance A/D converter with 125 MHz sampling rate converts signals received on RXP/RXN pins to 6 bits data streams; besides it possess auto-gain-control capability that will further improve receiving performance especially under long cable or harsh detrimental signal integrity. Due to high pass characteristic on transformer, built in base-line-wander correcting circuit will cancel it out and restore its DC level.

3.2.2.2 Adaptive Equalizer and Timing Recovery Module

All digital design is especial immune from noise environments and achieves better correlation between production and system testing. Baud rate Adaptive Equalizer/Timing Recovery compensates line loss induced from twisted pair and tracks far end clock at 125M samples per second. Adaptive Equalizer implemented with Feed forward and Decision Feedback techniques meet the requirement of BER less than 10-12 for transmission on CAT5 twisted pair cable ranging from 0 to 120 meters.

3.2.2.3 NRZI/NRZ and Serial/Parallel Decoder

The recovered data is converted from NRZI to NRZ. The data is not necessarily aligned to 4B/5B code group's boundary.

3.2.2.4 Data De-scrambling

The de-scrambler acquires synchronization with the data stream by recognizing idle bursts of 40 or more bits and locking its deciphering Linear Feedback Shift Register (LFSR) to the state of the scrambling LFSR. Upon achieving synchronization, the incoming data is XORed by the deciphering LFSR and de-scrambled.

In order to maintain synchronization, the de-scrambler continuously monitors the validity of the unscrambled data that it generates. To ensure this, a link state monitor and a hold timer are used to constantly monitor the synchronization status. Upon synchronization of the de-scrambler the hold timer starts a 722 us countdown. Upon detection of sufficient idle symbols within the 722 us period, the hold timer will reset and begin a new countdown. This monitoring operation will continue indefinitely given a properly operating network connection with good signal integrity. If the link state monitor does not recognize sufficient unscrambled idle symbols within 722 us period, the de-scrambler will be forced out of the current state of synchronization and reset in order to re-acquire synchronization.

3.2.2.5 Symbol Alignment

The symbol alignment circuit in the ADM6999G/GX determines code word alignment by recognizing the /J/K delimiter pair. This circuit operates on unaligned data from the de-scrambler. Once the /J/K symbol pair (11000 10001) is detected, subsequent data is aligned on a fixed boundary.

3.2.2.6 Symbol Decoding

The symbol decoder functions as a look-up table that translates incoming 5B symbols into 4B nibbles. The symbol decoder first detects the /J/K symbol pair preceded by idle symbols and replaces the symbol with MAC preamble. All subsequent 5B symbols are converted to the corresponding 4B nibbles for the duration of the entire packet. This conversion ceases upon the detection of the /T/R symbol pair denoting the end of stream delimiter (ESD). The translated data presented on the internal RXD[3:0] signal lines with RXD[0] represents the least significant bit of the translated nibble.

3.2.2.7 Valid Data Signal

The valid data signal (RXDV) indicates that recovered and decoded nibbles are being presented on the internal RXD[3:0] synchronous to receive clock, RXCLK. RXDV is asserted when the first nibble of translated /J/K is ready for transfer over the internal MII. It remains active until either the /T/R delimiter is recognized, link test indicates failure, or no signal is detected. On any of these conditions, RXDV is de-asserted.

3.2.2.8 Receive Errors

The RXER signal is used to communicate receiver error conditions. While the receiver is in a state of holding RXDV asserted, the RXER will be asserted for each code word that does not map to a valid code-group.

3.2.2.9 100Base-X Link Monitor

The 100Base-X link monitor function allows the receiver to ensure that reliable data is being received. Without reliable data reception, the link monitor will halt both transmitting and receiving operations until such time that a valid link is detected.

The ADM6999G/GX performs the link integrity test as outlined in IEEE 100Base-X (Clause 24) link monitor state diagram. The link status is multiplexed with 10Mbits/s link status to form the reportable link status bit in serial management register 1_H, and driven to the LNKACT pin.

When persistent signal energy is detected on the network, the logic moves into a Link-Ready state after approximately 500 μs, and waits for an enable from the auto negotiation module. When receiving, the link-up state is entered, and the transmission and reception logic blocks become active. Should auto negotiation be disabled, the link integrity logic moves immediately to the link-up state after entering the link-ready state.

3.2.2.10 Carrier Sense

Carrier sense (CRS) for 100Mbits/s operation is asserted upon the detection of two noncontiguous zeros occurring within any 10-bit boundary of the received data stream.

The carrier sense function is independent of symbol alignment. In switch mode, CRS is asserted during either packet transmission or reception. For repeater mode, CRS is asserted only during packet reception. When the idle symbol pair is detected in the received data stream, CRS is de-asserted. In repeater mode, CRS is only asserted due to receive activity. CRS is intended to encapsulate RXDV.

3.2.2.11 Bad SSD Detection

A bad start of stream delimiter (Bad SSD) is an error condition that occurs in the 100Base-X receiver if carrier is detected (CRS asserted) and a valid /J/K set of code-group (SSD) is not received.

If this condition is detected, then the ADM6999G/GX will assert RXER and present RXD[3:0] = 1110 to the internal MII for the cycles corresponding to the received 5B code-groups until at least two idle code-groups are detected. Once at least two idle code groups are detected, RXER and CRS become de-asserted.

3.2.2.12 Far-End Fault

Auto negotiation provides a mechanism for transferring information from the Local Station to the link Partner that a remote fault has occurred for 100Base-TX. As auto negotiation is not currently specified for the operation over fiber, the far end fault indication function (FEFI) provides this capability for 100Base-FX applications.

A remote fault is an error in the link that one station can detect while the other cannot. An example of this is a disconnected wire at a station's transmitter. This station will be receiving valid data and detect that the link is good via the link integrity monitor, but will not be able to detect that its transmission is not propagating to the other station.

A 100Base-FX station that detects such a remote fault may modify its transmitted idle stream from all ones to a group of 84 ones followed by a single 0. This is referred to as the FEFI idle pattern.

3.2.3 100Base-TX Transceiver

ADM6999G/GX implements a TP-PMD compliant transceiver for 100Base-TX operation. The differential transmitting driver is shared by the 10Base-T and 100Base-TX subsystems. This arrangement results in one device that uses the same external magnetic for both the 10Base-T and the 100Base-TX transmissions with simple RC component connections. The individually wave-shaped 10Base-T and 100Base-TX transmitting signals are multiplexed in the transmission output driver selection.

3.2.3.1 Transmit Drivers

The ADM6999G/GX 100Base-TX transmission driver implements MLT-3 translation and wave-shaping functions. The rise/fall time of the output signal is closely controlled to conform to the target range specified in the ANSI TP-PMD standard.

3.2.3.2 Twisted-Pair Receiver

For 100Base-TX operation, the incoming signal is detected by the on-chip twisted-pair receiver that consists of a differential line receiver, an adaptive equalizer and a base-line wander compensation circuits.

The ADM6999G/GX uses an adaptive equalizer that changes filter frequency response in accordance with cable length. The cable length is estimated based on the incoming signal strength. The equalizer tunes itself automatically for any cable length to compensate for the amplitude and phase distortions incurred from the cable.

3.2.4 10Base-T Module

The 10Base-T Transceiver Module is IEEE 802.3 compliant. It includes the receiver, transmitter, collision, heartbeat, loop back, jabber, wave shaper, and link integrity functions, as defined in the standard.

The ADM6999G/GX 10Base-T module is comprised of the following functional blocks:

- Manchester encoder and decoder
- Collision detector
- Link test function
- Transmit driver and receiver
- Serial and parallel interface
- Jabber and SQE test functions
- Polarity detection and correction

3.2.4.1 Operation Modes

The ADM6999G/GX 10Base-T module is capable of operating in either half-duplex mode or full-duplex mode. In half-duplex mode, the ADM6999G/GX functions as an IEEE 802.3 compliant transceiver with fully integrated filtering. The COL signal is asserted during collisions or jabber events, and the CRS signal is asserted during transmitting and receiving. In full duplex mode the ADM6999G/GX can simultaneously transmit and receive data.

3.2.4.2 Manchester Encoder/Decoder

Data encoding and transmission begin when the transmission enable input (TXEN) goes high and continue as long as the transceiver is in good link state. Transmission ends when the transmission enable input goes low. The last transition occurs at the center of the bit cell if the last bit is a 1, or at the boundary of the bit cell if the last bit is 0.

Decoding is accomplished by a differential input receiver circuit and a phase-locked loop that separate the Manchester-encoded data stream into clock signals and NRZ data. The decoder detects the end of a frame when no more mid bit transitions are detected. Within one and half bit times after the last bit, carrier sense is de-asserted.

3.2.4.3 Transmit Driver and Receiver

The ADM6999G/GX integrates all the required signal conditioning functions in its 10Base-T block such that external filters are not required. Only one isolation transformer and impedance matching resistors are needed for the 10Base-T transmitting and receiving interface. The internal transmitting filter ensures that all the harmonics in the transmission signal are attenuated properly.

3.2.4.4 Smart Squelch

The smart squelch circuit is responsible for determining when valid data is present on the differential reception. The ADM6999G/GX implements an intelligent receiving squelch on the RXP/RXN differential inputs to ensure that impulse noise on the receiving inputs will not be mistaken for a valid signal. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10Base-T standard) to determine the validity of data on the twisted-pair inputs.

The signal at the start of the packet is checked by the analog squelch circuit and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly, the opposite squelch level must then be exceeded within 150ns. Finally, the signal must exceed the original squelch level within an additional 150ns to ensure that the input waveform will not be rejected.

Only after all these conditions have been satisfied a control signal will be generated to indicate the remainder of the circuitry that valid data is present.

Valid data is considered to be present until the squelch level has not been generated for a time longer than 200 ns, indicating end of packet. Once good data has been detected, the squelch levels are reduced to minimize the effect

of noise, causing premature end-of-packet detection. The receiving squelch threshold level can be lowered for use in longer cable applications. This is achieved by setting bit 10 of register address 11_H.

3.2.5 Carrier Sense

Carrier Sense (CRS) is asserted due to receive activity once valid data is detected via the smart squelch function. For 10 Mbits/s half duplex operation, CRS is asserted during either packet transmission or reception. For 10 Mbits/s full duplex and repeater mode operations, the CRS is asserted only due to receive activity.

3.2.6 Jabber Function

The jabber function monitors the ADM6999G/GX output and disables the transmitter if it attempts to transmit a longer than legal sized packet. If TXEN is high for greater than 24ms, the 10Base-T transmitter will be disabled. Once disabled by the jabber function, the transmitter stays disabled for the entire time that the TXEN signal is asserted. This signal has to be de-asserted for approximately 256 ms (The un-jab time) before the jabber function re-enables the transmit outputs. The jabber function can be disabled by programming bit 4 of register address 10_H to high.

3.2.7 Link Test Function

A link pulse is used to check the integrity of the connection with the remote end. If valid link pulses are not received, the link detector disables the 10Base-T twisted-pair transmitter, receiver, and collision detection functions.

The link pulse generator produces pulses as defined in IEEE 802.3 10Base-T standard. Each link pulse is nominally 100ns in duration and is transmitted every 16 ms, in the absence of transmit data.

3.2.8 Automatic Link Polarity Detection

ADM6999G/GX's 10Base-T transceiver module incorporates an "automatic link polarity detection circuit". The inverted polarity is determined when seven consecutive link pulses of inverted polarity or three consecutive packets are received with inverted end-of-packet pulses. If the input polarity is reversed, the error condition will be automatically corrected and reported in bit 5 of register 10_H.

3.2.9 Clock Synthesizer

The ADM6999G/GX implements a clock synthesizer that generates all the reference clocks needed from a single external frequency source. The clock source must be a TTL level signal at 25 MHz +/- 50ppm

3.2.10 Auto Negotiation

The Auto Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operations supported by both devices. Fast Link Pulse (FLP) Bursts provide the signaling used to communicate auto negotiation abilities between two devices at each end of a link segment. For further details regarding auto negotiation, refer to Clause 28 of the IEEE 802.3u specification. The ADM6999G/GX supports four different Ethernet protocols, so the inclusion of auto negotiation ensures that the highest performance protocol will be selected based on the ability of the link partner.

Highest priority relative to the following list:

1. 100Base-TX full duplex (highest priority)
2. 100Base-TX half duplex
3. 10Base-T full duplex
4. 10Base-T half duplex (lowest priority)

3.3 Memory Block Description

ADM6999G/GX builds in 768K bits memory inside. Memory buffer is divided in two blocks. One is MAC addressing table and another one is data buffer.

MAC address Learning Table size is 2048 entries with each entry occupying eight bytes length. These eight bytes data include 6 bytes source address, VLAN information, Port information and Aging counter.

Data buffer is divided into 512 bytes/block. ADM6999G/GX buffer management is fixed block number for each port and all port share one global buffer. This architecture can get better memory utilization and network balance on different speed and duplex test conditions.

Received packet will be separate in several 512 bytes/block and chain together. If the packet size is more than 512 bytes then ADM6999G/GX will chain two or more blocks to store receiving packet.

3.4 Switch Functional Description

The ADM6999G/GX uses a “store & forward” switching approach for the following reason:

Store & forward switches allow switching between different speed media (e.g. 10BaseX and 100BaseX). Such switches require the large elastic buffer especially bridging between a server on a 100Mbps network and clients on a 10Mbps segment.

Store & forward switches improve overall network performance by acting as a “network cache”

Store & forward switches prevent the forwarding of corrupted packets by the frame check sequence (FCS) before forwarding to the destination port.

3.4.1 Basic Operation

The ADM6999G/GX receives incoming packets from one of its ports, searches in the Address Table for the Destination MAC Address and then forwards the packet to the other port within the same VLAN group, if appropriate. If the destination address is not found in the address table, the ADM6999G/GX treats the packet as a broadcast packet and forwards the packet to the other ports within the same VLAN group.

The ADM6999G/GX automatically learns the port number of attached network devices by examining the Source MAC Address of all incoming packets at wire speed. If the Source Address is not found in the Address Table, the device adds it to the table.

3.4.1.1 Address Learning

The ADM6999G/GX uses a hash algorithm to learn the MAC address and can learn up to 2K MAC addresses. Address is stored in the Address Table. The ADM6999G/GX searches for the Source Address (SA) of an incoming packet in the Address Table and acts as below:

If the SA was not found in the Address Table (a new address), the ADM6999G/GX waits until the end of the packet (non-error packet) and updates the Address Table. If the SA was found in the Address Table, then aging value of each corresponding entry will be reset to 0.

When the DA is PAUSE command, the learning process will be disabled automatically by ADM6999G/GX.

3.4.1.2 Address Recognition and Packet Forwarding

The ADM6999G/GX forwards the incoming packets between bridged ports according to the Destination Address (DA) as below. All the packet forwarding will check VLAN first. A forwarding port must be within the same VLAN as the source port.

1. If the DA is an UNICAST address and the address was found in the Address Table, the ADM6999G/GX will check the port number and acts as follows:
   a) If the port number is equal to the port on which the packet was received, the packet is discarded.
   b) If the port number is different, the packet is forwarded across the bridge.

2. If the DA is an UNICAST address and the address was not found, the ADM6999G/GX treats it as a multicast packet and forwards across the bridge.
3. If the DA is a Multicast address, the packet is forwarded across the bridge.
4. If the DA is PAUSE Command (01-80-C2-00-00-01), then this packet will be dropped by ADM6999G/GX. ADM6999G/GX can issue and learn PAUSE command.
5. ADM6999G/GX will forward the packet with DA of (01-80-C2-00-00-00), filter out the packet with DA of (01-80-C2-00-00-01), and forward the packet with DA of (01-80-C2-00-00-02 ~ 01-80-C2-00-00-0F)

3.4.1.3 Address Aging

Address aging is supported for topology changes such as an address moving from one port to the other. When this happens, the ADM6999G/GX internally has a 300 seconds timer and will age out (remove) the address from the address table. Aging function can be enabled/disabled by users. Normally, disabling aging function is for security purpose.

3.4.1.4 Back off Algorithm

The ADM6999G/GX implements the truncated exponential back off algorithm compliant to the IEEE802.3 CSMA/CD standard. ADM6999G/GX will restart the back off algorithm by choosing 0-9 collision counts. The ADM6999G/GX resets the collision counter after 16 consecutive retransmit trials.

3.4.1.5 Inter-Packet Gap (IPG)

IPG is the idle time between any two successive packets from the same port. The typical number is 96-bits time. The value is 9.6μs for 10Mbps ETHERNET, and 960ns for 100Mbps fast ETHERNET. ADM6999G/GX provides the option of a 92-bit gap in EEPROM to prevent packet loss when Flow Control is turned off and clock P.P.M. values differ.

3.4.1.6 Illegal Frames

The ADM6999G/GX will discard all illegal frames such as small packets (less than 64 bytes), oversized packets (greater than 1518 or 1522 bytes) and bad CRC. Dribbling packing with good CRC value will be accepted by ADM6999G/GX. In case of bypass mode is enabled, ADM6999G/GX will support tagged and untagged packets with size up to 1522 bytes. In case of non-bypass mode, ADM6999G/GX will support tagged packets up to 1526bytes, and untagged packets up to 1522bytes.

3.4.1.7 Half Duplex Flow Control

Back Pressure function is supported for half-duplex operation. When the ADM6999G/GX cannot allocate a receiving buffer for an incoming packet (buffer full), the device will transmit a jam pattern on the port, thus forcing a collision. Back Pressure is enabled by the BPEN set during RESET asserting. An Infineon-ADMtek Co Ltd proprietary algorithm is implemented inside the ADM6999G/GX to prevent back pressure function causing HUB partitioned under heavy traffic environment and reduce the packet lost rate to increase the whole system performance.

3.4.1.8 Full Duplex Flow Control

When full duplex port runs out of its receiving buffer, a PAUSE packet command will be issued by ADM6999G/GX to notice the packet sender to pause transmission. This frame based flow control is totally compliant to IEEE 802.3x. ADM6999G/GX can issue or receive pause packet.

3.4.1.9 Broadcast Storm Filter

If Broadcast Storming filter is enable, the broadcast packets over the rising threshold within 50 ms will be discarded by the threshold setting. See EEPROM Reg.10_H.

Broadcast storm mode after initial:

Time interval: 50 ms

The max. packet number = 7490 in 100Base, 749 in 10Base

Table 4 Port Rising/Falling Threshold

Per Port Rising Threshold				
	00	01	10	11
All 100TX	Disable	10%	20%	40%
Not All 100TX	Disable	1%	2%	4%

Per Port Falling Threshold				
	00	01	10	11
All 100TX	Disable	5%	10%	20%
Not All 100TX	Disable	0.5%	1%	2%

3.4.2 Auto TP MDIX Function

At normal application which Switch connects to NIC card is by one by one TP cable. If Switch connects to other devices such as another Switch must be by two way. The first one is Cross Over TP cable. The second way is to use extra RJ45 which crossover internal TX+- and RX+- signal. By second way customers can use one by one cable to connect two Switch devices. All these efforts need extra costs and are not good solutions. ADM6999G/GX provides Auto MDIX function which can adjust TX+- and RX+- at correct pin. Users can use one by one cable between ADM6999G/GX and other devices. This function can be Enable/Disable by hardware pin and EEPROM configuration register 01_H~09_H bit 15. If hardware pin sets all ports at Auto MDIX mode then EEPROM setting is useless. If the hardware pin sets all ports at non Auto MDIX mode then EEPROM can set each port's Auto MDIX function to be enabled or disabled.

3.4.3 Port Locking

Port locking function will provide customers a simple way to limit per port's user to one. If this function is turned on then ADM6999G/GX will lock first MAC address in learning table. After this MAC address locking will never age out except Reset signal. Another MAC address which is not the same as the locking one will be dropped. ADM6999G/GX provides one MAC address per port. This function is per-port-setting. When turning on Port Locking function, we recommend customers to turn off aging function. See EEPROM register 12_H bit 0~8.

3.4.4 VLAN Setting & Tag/Untag & Port-base VLAN

ADM6999G/GX supports bypass mode and untagged port as default setting while the chip is power-on. Thus, every packet with or without tag will be forwarding to the destination port without any modification by ADM6999G/GX. Meanwhile port-base VLAN could be enabled according to the PVID value (user define 4bits to map 16 groups written at register 13_H to register 22_H) of the configuration content of each port.

ADM6999G/GX also supports 16 802.1Q VLAN groups. In VLAN four bytes tag include twelve VLAN ID. ADM6999G/GX learns user defined four bits of VID. If users need to use this function, two EEPROM registers are needed to be programmed first:

- Port VID number at EEPROM register 01_H~09_H bit 13~10, register 28_H~$2B_H$ and register $2C_H$ bit 7~0: ADM6999G/GX will check coming packet. If coming packet is non VLAN packet then ADM6999G/GX will use PVID as VLAN group reference. ADM6999G/GX will use packet's VLAN value when receive tagged packet.
- VLAN Group Mapping Register. EEPROM register 013_H~022_H defines VLAN grouping value. Users use these register to define VLAN group.

Users can define each port as Tagged port or Untagged port by Configuration register Bit 4. The operation of packets between Tagged port and Untagged port can be explained by following example:

Example1: Port receives Untagged packet and send to Untagged port

ADM6999G/GX will check the port user define four bits of VLAN ID first then check VLAN group register. If the destination port is in the same VLAN as the receiving port then this packet will forward to the destination port without any change. If the destination port is not in the same VLAN as the receiving port then this packet will be dropped.

Example2: Port receives Untagged packet and send to Tagged port

ADM6999G/GX will check the port user define fours bits of VLAN ID first then check VLAN group register. If the destination port is the same VLAN as the receiving port than this packet will forward to destination port with four byte VLAN Tag and new CRC. If the destination port is not the same VLAN as receiving port then this packet will be dropped.

Example3: Port receives Tag packet and send to Untag port

ADM6999G/GX will check the packet VLAN ID first then check VLAN group register. If the destination port is the same VLAN as receiving port than this packet will forward to destination port after removing four bytes with new CRC error. If the destination port is not the same VLAN as receiving port then this packet will be dropped.

Example4: Port receives Tag packet and send to Tag port

ADM6999G/GX will check the user define packet VLAN ID first then check VLAN group register. If the destination port is the same VLAN as receiving port than this packet will forward to destination port without any change. If the destination port is not the same VLAN as receiving port then this packet will be dropped.

3.4.5 Priority Setting

It is a trend that data, voice and video will be put on networking, Switch not only deals data packets but also provides services of multimedia data. ADM6999G/GX provides two priority queues on each port with N:1 rate. See EEPROM Reg. 10_H.

This priority function can be set by three ways as below:

- By Port Base: Set specific port at specific queue. ADM6999G/GX only checks the port priority and does not check packet's content VLAN and TOS at bypass mode.
- By VLAN first: ADM6999G/GX checks VLAN three priority bit first then IP TOS priority bits. The chip must be set as Tagged mode.
- By IP TOS first: ADM6999G/GX checks IP TOS three priority bit first then VLAN three priority bits. Chip must be set as Tagged mode.

If the port sets as VLAN/TOS priority but the receiving packet is without VLAN or TOS information then port base priority will be used.

3.4.6 LED Display

The ADM6999G/GX provides two different interfaces to drive the status to the LEDs. Each interface supports visibility of each port's speed, combines transmitting and receiving activity, and duplex collision status. Different interfaces and its color mode are applied according to LEDMODE pin and the configuration of the ADM6999G/GX latched during the power on reset.

Table 5 LED Display

Configuration		LED Mode	Interface utilized
ADM6999G /GX	8+1 GMII	1: Dual Color0: Single Color	Serial Interface: Totally two pins, LEDCLK, and LEDDATA are used to output the LED status.

3.4.6.1 Serial LED Interface

A two pins interface, LEDDATA and LEDCLK, provides external shift register to capture the LED status indicated by the ADM6999G/GX. The status is encapsulated within the shift sequence, which is a consecutive stream of 8-bit status words. The first word is the DUPCOL status, the second is the speed status, and the last is the LNKACT status. Each word contains 8 bits and each bit corresponds to each port of the designated LED status. The designated LED status is sent first followed by port1 then port 2, etc.. The shift sequence is repeated every 40 ms and each bit last 640ns. **Figure 3** shows the external circuit.

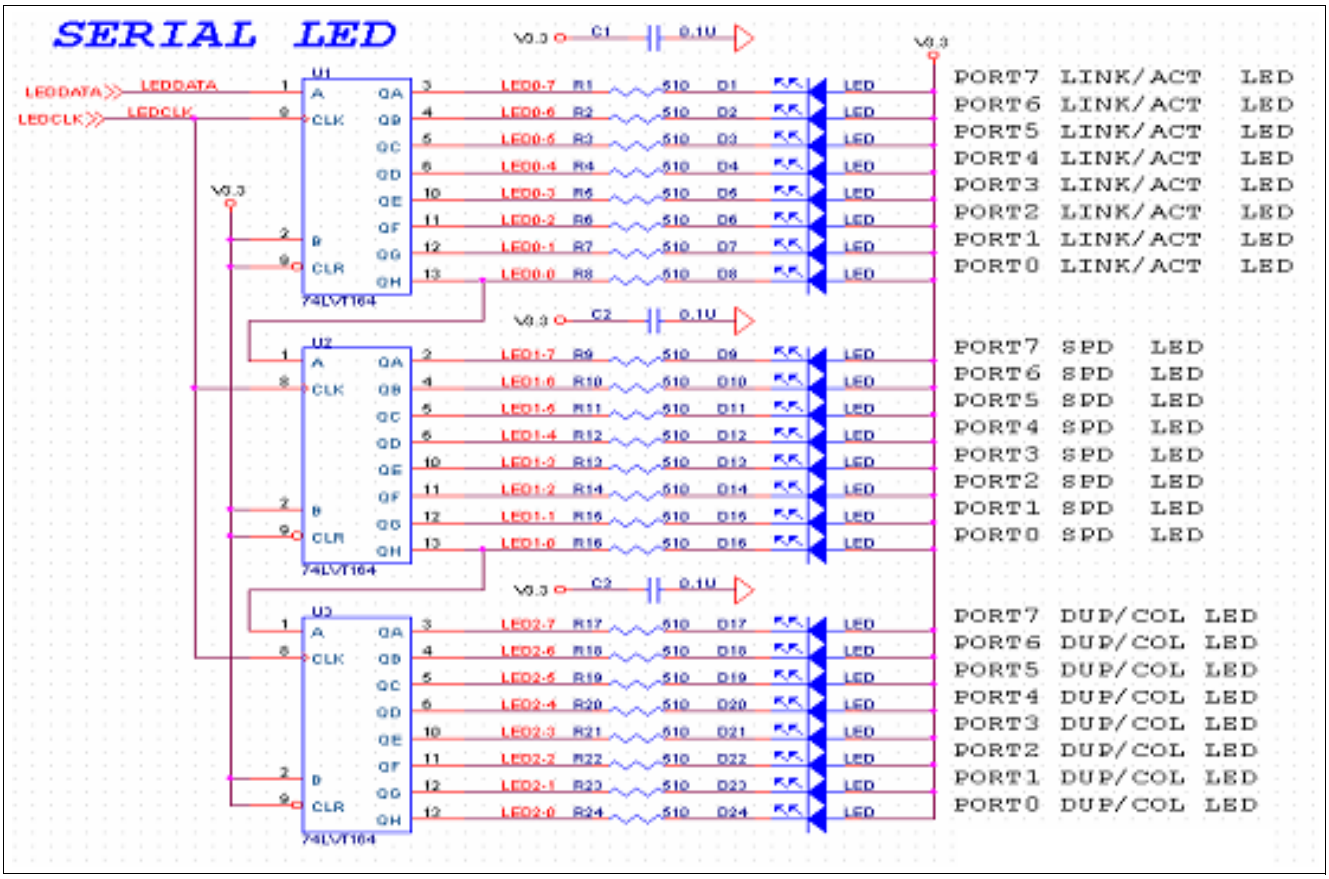


Figure 3 Serial LED Interface

3.4.6.2 LED Display Mode

Three LED per port are provided by ADM6999G/GX. Link/Act, Duplex/Col & Speed are three LED display of ADM6999G/GX. Dual color LED mode is also supported by ADM6999G/GX. For easy production purpose ADM6999G/GX will send test signals to each LED at power on reset stage. EEPROM register 12_H defines LED configuration table.

ADM6999G/GX LED is active Low signal. Dupcol0 & Dupcol1 will check external signal at Reset time. If external signal adds a pull high resister then LED will be active Low. If external signal adds a pull down resister then LED will drive high.

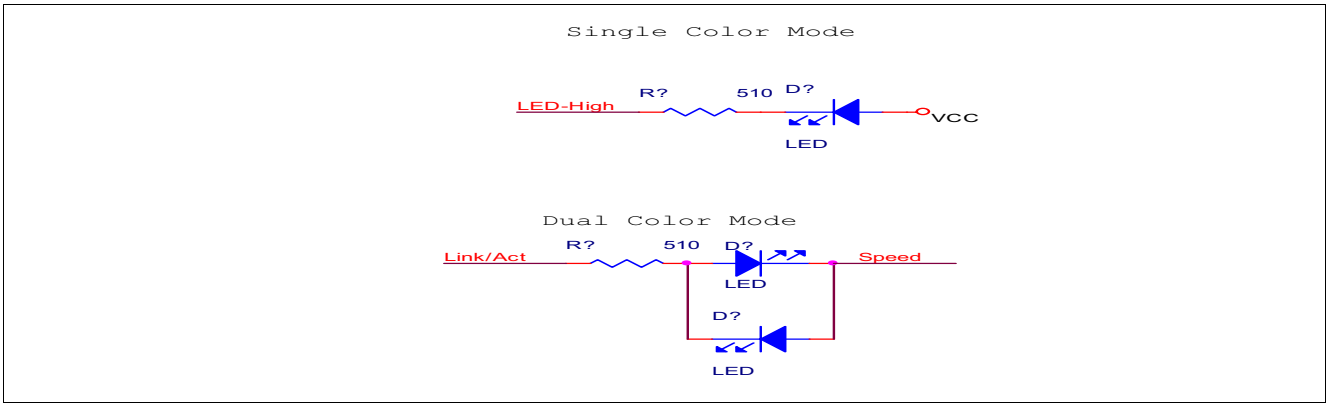


Figure 4 LED Display Mode

3.5 EEPROM Content

EEPROM provides ADM6999G/GX many options setting such as:

- Port Configuration: Speed, Duplex, Flow Control Capability and Tag/Untag
- VLAN & TOS Priority Mapping
- Broadcast Storming rate and Trunk
- Fiber Select, Auto MDIX select
- VLAN Mapping
- Per Port Buffer number

Table 6 EEPROM Map

Register	Bit 15-8	Bit 7-0	Default Value
00_H	Signature		4154_H
01_H	Port 0 Configuration		$040F_H$
02_H	Port 1 Configuration		$040F_H$
03_H	Port 2 Configuration		$040F_H$
04_H	Port 3 Configuration		$040F_H$
05_H	Port 4 Configuration		$040F_H$
06_H	Port 5 Configuration		$040F_H$
07_H	Port 6 Configuration		$040F_H$
08_H	Port 7 Configuration		$040F_H$
09_H	Expansion Port Configuration		$040F_H$
$0A_H$	VID 0,1 option	Giga port Configuration	5902_H
$0B_H$	Configuration Regsiter		8000_H
$0C_H$	Reserved		$FA50_H$
$0D_H$	Port 8 MII Data High		$FA50_H$
$0E_H$	VLAN priority Map High	VLAN priority Map Low	5500_H
$0F_H$	TOS priority Map High	TOS priority Map Low	5500_H
10_H	Miscellaneous Configuration 0		0040_H
11_H	Miscellaneous Configuration 1		$FF00_H$
12_H	Miscellaneous Configuration 2		3600_H
13_H	VLAN 0 outbound Port Map or VLAN 1 outbound Port Map	VLAN 0 outbound Port Map or VLAN 0 outbound Port Map	$FFFF_H$
14_H	VLAN 1 outbound Port Map or VLAN 3 outbound Port Map	VLAN 1 outbound Port Map or VLAN 2 outbound Port Map	$FFFF_H$
15_H	VLAN 2 outbound Port Map or VLAN 5 outbound Port Map	VLAN 2 outbound Port Map or VLAN 4 outbound Port Map	$FFFF_H$
16_H	VLAN 3 outbound Port Map or VLAN 7 outbound Port Map	VLAN 3 outbound Port Map or VLAN 6 outbound Port Map	$FFFF_H$
17_H	VALN 4 outbound Port Map or VLAN 9 outbound Port Map	VLAN 4 outbound Port Map or VLAN 8 outbound Port Map	$FFFF_H$

Table 6 EEPROM Map (cont'd)

Register	Bit 15-8	Bit 7-0	Default Value
18_H	VLAN 5 outbound Port Map or VLAN 11 outbound Port Map	VLAN 5 outbound Port Map or VLAN 10 outbound Port Map	$FFFF_H$
19_H	VLAN 6 outbound Port Map or VLAN 13 outbound Port Map	VLAN 6 outbound Port Map or VLAN 12 outbound Port Map	$FFFF_H$
$1A_H$	VLAN 7 outbound Port Map or VLAN 15 outbound Port Map	VLAN 7 outbound Port Map or VLAN 14 outbound Port Map	$FFFF_H$
$1B_H$	VLAN 8 outbound Port Map or VLAN 17 outbound Port Map	VLAN 8 outbound Port Map or VLAN 16 outbound Port Map	$FFFF_H$
$1C_H$	VLAN 9 outbound Port Map or VLAN 19 outbound Port Map	VLAN 9 outbound Port Map or VLAN 18 outbound Port Map	$FFFF_H$
$1D_H$	VLAN 10 outbound Port Map or VLAN 21 outbound Port Map	VLAN 10 outbound Port Map or VLAN 20 outbound Port Map	$FFFF_H$
$1E_H$	VLAN 11 outbound Port Map or VLAN 23 outbound Port Map	VLAN 11 outbound Port Map or VLAN 22 outbound Port Map	$FFFF_H$
$1F_H$	VLAN 12 outbound Port Map or VLAN 25 outbound Port Map	VLAN 12 outbound Port Map or VLAN 24 outbound Port Map	$FFFF_H$
20_H	VLAN 13 outbound Port Map or VLAN 27 outbound Port Map	VLAN 13 outbound Port Map or VLAN 26 outbound Port Map	$FFFF_H$
21_H	VLAN 14 outbound Port Map or VLAN 29 outbound Port Map	VLAN 14 outbound Port Map or VLAN 28 outbound Port Map	$FFFF_H$
22_H	VLAN 15 outbound Port Map or VLAN 31 outbound Port Map	VLAN 15 outbound Port Map or VLAN 30 outbound Port Map	$FFFF_H$
23_H	P1 Buffer Threshold Control	P0 Buffer Threshold Control	0000_H
24_H	P3 Buffer Threshold Control	P2 Buffer Threshold Control	0000_H
25_H	P5 Buffer Threshold Control	P4 Buffer Threshold Control	0000_H
26_H	P7 Buffer Threshold Control	P6 Buffer Threshold Control	0000_H
27_H	Total Buffer Threshold Control	P8 Buffer Threshold Control	0000_H
28_H	P1 PVID [11:4]	P0 PVID [11:4]	0000_H
29_H	P3 PVID [11:4]	P2 PVID [11:4]	0000_H
$2A_H$	P5 PVID [11:4]	P4 PVID [11:4]	0000_H
$2B_H$	P7 PVID [11:4]	P6 PVID [11:4]	0000_H
$2C_H$	VLAN Group Configuration	P8 PVID [11:4]	$D000_H$
$2D_H$	Reserved		4442_H

3.5.1 EEPROM Registers Overview

Table 7 Registers Address SpaceRegisters Address Space

Module	Base Address	End Address	Note
EEPROM	00_H	$2C_H$	

Table 8 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
SR	Signature Register	00_H	**33**
PCR_0	Port Configuration Register 0	01_H	**34**
PCR_1	Port 1 Configuration Register	02_H	**35**
PCR_2	Port 2 Configuration Register	03_H	**35**
PCR_3	Port 3 Configuration Register	04_H	**35**
PCR_4	Port 4 Configuration Register	05_H	**35**
PCR_5	Port 5 Configuration Register	06_H	**35**
PCR_6	Port 6 Configuration Register	07_H	**35**
PCR_7	Port 7 Configuration Register	08_H	**35**
PCR_8	Port 8 Configuration Register	09_H	**35**
GPCR	Gigabit Port Configuration Register	$0A_H$	**36**
CR	Configuration Register	$0B_H$	**37**
Res	Reserved Register	$0C_H$	**38**
PMII	Port 8 MII write data	$0D_H$	**39**
VLAN_PMR	VLAN Priority Map Register	$0E_H$	**40**
TOS_PMR	TOS Priority Map Register	$0F_H$	**41**
MCR_0	Miscellaneous Configuration Register 0	10_H	**43**
VLAN_MSR	VLAN Mode Select Register	11_H	**45**
MCR_2	Miscellaneous Configuration Register 2	12_H	**48**
VLAN_MTR_0	VLAN Mapping Table Register 0	13_H	**49**
VLAN_MTR	VLAN Mapping Table Registers	13_H	**50**
VLAN_MTR_1	VLAN Mapping Table Register 1	14_H	**51**
VLAN_MTR_2	VLAN Mapping Table Register 2	15_H	**51**
VLAN_MTR_3	VLAN Mapping Table Register 3	16_H	**51**
VLAN_MTR_4	VLAN Mapping Table Register 4	17_H	**51**
VLAN_MTR_5	VLAN Mapping Table Register 5	18_H	**51**
VLAN_MTR_6	VLAN Mapping Table Register 6	19_H	**51**
VLAN_MTR_7	VLAN Mapping Table Register 7	$1A_H$	**51**
VLAN_MTR_8	VLAN Mapping Table Register 8	$1B_H$	**51**
VLAN_MTR_9	VLAN Mapping Table Register 9	$1C_H$	**51**
VLAN_MTR_10	VLAN Mapping Table Register 10	$1D_H$	**51**
VLAN_MTR_11	VLAN Mapping Table Register 11	$1E_H$	**51**
VLAN_MTR_12	VLAN Mapping Table Register 12	$1F_H$	**51**
VLAN_MTR_13	VLAN Mapping Table Register 13	20_H	**51**

Table 8 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
VLAN_MTR_14	VLAN Mapping Table Register 14	21_H	51
VLAN_MTR_15	VLAN Mapping Table Register 15	22_H	51
PBTCR_P01	Port Buffer Threshold Control Reg. P0, P1	23_H	52
PBTCR_P23	Port Buffer Threshold Control Reg. P2, P3	24_H	52
PBTCR_P45	Port Buffer Threshold Control Reg. P4, P5	25_H	53
PBTCR_P67	Port Buffer Threshold Control Reg. P6, P7	26_H	53
TBTCR	Total Buffer Threshold Control Register	27_H	54
PVID11_4_CR_P01	Port0, 1 PVID bit11~4 Configuration Register	28_H	55
PVID11_4_CR_P23	Port2, 3 PVID bit11~4 Configuration Register	29_H	56
PVID11_4_CR_P45	Port4, 5 PVID bit 11~4 Configuration Register	$2A_H$	57
PVID11_4_CR_P67	Port6, 7 PVID bit 11~4 Configuration Register	$2B_H$	58
PVID11_4_VLAN_CR	P8 PVID bit 11~4/VLAN Group Shift Bits Conf.	$2C_H$	58

The register is addressed wordwise.

Table 9 Register Access Types

Mode	Symbol	Description HW	Description SW
read/write	rw	Register is used as input for the HW	Register is readable and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latches high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latches high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latches high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latches high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiates the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiates the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiates the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiates the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared

Table 9 Register Access Types (cont'd)

Mode	Symbol	Description HW	Description SW
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is readable and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is readable and writable by SW.

Table 10 Registers Clock DomainsRegisters Clock Domains

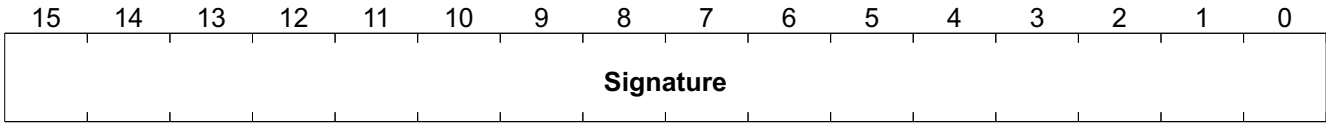
Clock Short Name	Description

3.5.1.1 EEPROM Registers Description

Signature Register

ADM6999G/GX will check register 0 value before read all EEPROM content. If this value does not match with 4154_H then other values in EEPROM will be useless. ADM6999G/GX will use internal default value. Users can not write Signature register when programming ADM6999G/GX internal register.

SR	Offset	Reset Value
Signature Register	00_H	4154_H



Field	Bits	Type	Description
Signature	15:0	ro	**Signature** 4154_H, must be value

Configuration Registers

Register 09_H bit5 is not effective on disable port. User can disable port by VLAN.

PCR_0	Offset	Reset Value
Port Configuration Register 0	01_H	$040F_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANE	SI	ID				PBPN		EN	TOS	PD	TP	DC	SC	AN	FC

Field	Bits	Type	Description
ANE	15	rw	**Auto MDIX Enable** Hardware Reset latch value EECK can set global Auto MDIX function. If hardware pin sets all port at Auto MDIX then this bit is useless. If hardware pin sets chip at non Auto MDIX then this bit can set each port at Auto MDIX. 0_B **D**, disable, default 1_B **E**, enable
SI	14	rw	**Select FX Interface** Port7 TX/FX can be set by hardware Reset latch value P7FX. If hardware pin sets Port7 as FX then this bit is useless. If hardware pin sets Port7 as TX then this pin can set Port7 as FX or TX. 0_B **TP**, TP mode, default 1_B **FX**, FX mode
ID	13:10	rw	**Port VLAN ID** Check Register 28_H~$2C_H$ for other PVID[11:4]. 0001_B, Default
PBPN	9:8	rw	**Port Base Priority Number** From 1~0 mapping to Q1~Q0. 00_B , Default
EN	7	rw	**Enable Port Based Priority** If packet is without VLAN or TOS then port priority turnes on. If this bit turns on then ADM6999G/GX will not check TOS or VLAN as priority reference. ADM6999G/GX will check port base priority only. ADM6999G/GX's default is bypass mode which checks port base priority only. If user wants to check VLAN tagged priority then he must set chip at Tagged mode. See 11_H. 0_B , Disable, default 1_B , Enable
TOS	6	rw	**TOS Over VLAN Priority** Define ADM6999G/GX priority source when VLAN & TOS exists in the packet. 0_B , VLAN priority level higher than TOS, default 1_B , TOS priority level higher than VLAN

Field	Bits	Type	Description
PD	5	rw	**Port Disable** This function does not include Port8. Port8 can be disabled by VLAN separation. 0_B , enable port, default 1_B , disable port
TP	4	rw	**Output Packet Tagging** 0_B , Untagged port, default 1_B , Tagged port
DC	3	rw	**Duplex Capability** 0_B , Half Duplex 1_B , Full Duplex, default
SC	2	rw	**Speed Capability** 0_B , 10M 1_B , 100M, default
AN	1	rw	**Auto Negotiation Capability Enable** 0_B , disable 1_B , enable, default
FC	0	rw	**802.3X Flow Control Capability** 0_B , disable 1_B , enable, default

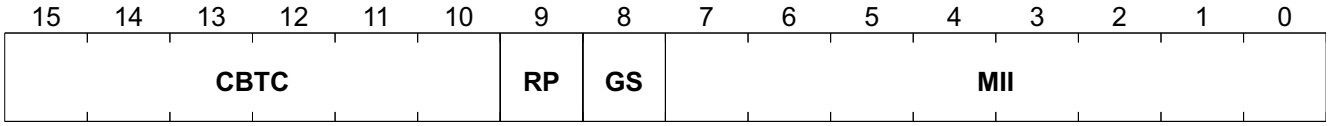
Table 11 PCR_x Registers Table

Register Short Name	Register Long Name	Offset Address	Page Number
PCR_1	Port 1 Configuration Register	02_H	
PCR_2	Port 2 Configuration Register	03_H	
PCR_3	Port 3 Configuration Register	04_H	
PCR_4	Port 4 Configuration Register	05_H	
PCR_5	Port 5 Configuration Register	06_H	
PCR_6	Port 6 Configuration Register	07_H	
PCR_7	Port 7 Configuration Register	08_H	
PCR_8	Port 8 Configuration Register	09_H	

Note: Register 09_H bit5 is not effective on disable port. User can disable port by VLAN

Gigabit Port Configuration Register

GPCR	Offset	Reset Value
Gigabit Port Configuration Register	$0A_H$	5902_H



Field	Bits	Type	Description
Res	15:10	ro	**Reserved.** 010110_B , default
RP	9	rw	**Replaced Packet VID 0, 1 by PVID** 1/ADM6999G/GX will replace packet VID by PVID when coming packet's VID=0 or1, 0/ADM6999G/GX will not replace packet's VID 0 & 1. 0_B , disable, default 1_B , enable
GS	8	rw	**Giga Speed selection MSB** Gigabit Speed selection MSB bit of MII register 01_H 1_B , default
MII	7:0	rw	**MII register 9 bit[15:8]** See MII register 09_H definition 20_H , default

Configuration Register

CR — **Configuration Register**

Offset $0B_H$

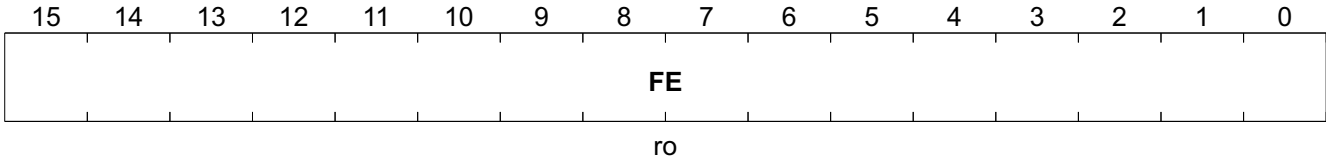
Reset Value 8000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE	Res	Res	Res					**ET**	**EL**	Res	Res				

Field	Bits	Type	Description
FE	15	rw	**Disable Far_End_Fault Detection** ADM6999G/GX will not recognize Far_End_Fault when turns on this bit. 0_B , enable 1_B , disable, default
Res	14	ro	**Reserved** 0_B , default
WE8	13	rw	**Port 8 MII Write Enable** High Active 0_B , default
RA8	12:8	rw	**Port 8 MII Register Address** If user wants to write data to Port8's PHY through MDC/MDIO then these five bits are MII register's address. 00000_B , default
ET	7	rw	**Enable Trunk** 0_B , Disable, default 1_B , enable Port6, 7 as Trunk port
EL	6	rw	**Enable IPG Leveling** 1/92 bit. 0/96 bit. When this bit is enable ADM6999G/GX will transmit packet out at 96 bit or 92 bit to clean buffer. If user disables this function then ADM6999G/GX will transmit packet at 96 bit. 0_B , Disable, default 1_B , Enable
Res	5	ro	**Reserved** 0_B , default
Res	4:0	ro	**Reserved** 00000_B , default

Reserved Register

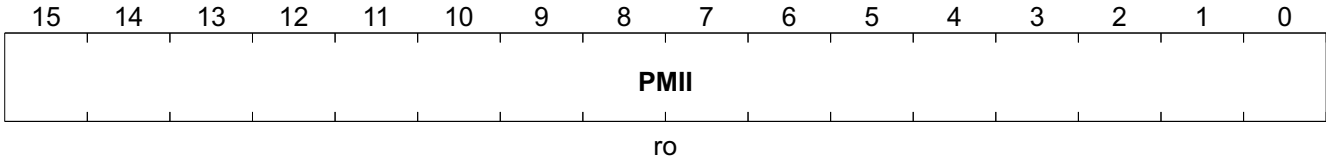
Res	Offset	Reset Value
Reserved Register	**$0C_H$**	**$FA50_H$**



Field	Bits	Type	Description
FE	15:0	ro	**Reserved**

Port 8 MII write data Register

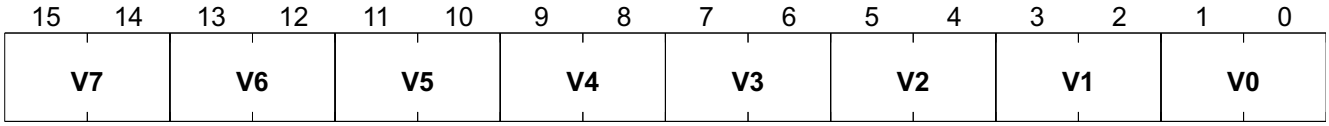
PMII	Offset	Reset Value
Port 8 MII write data	$0D_H$	$FA50_H$



Field	Bits	Type	Description
PMII	15:0	rw	**Port8 MII register write data** User can fill out write data for specific port8 MII register as assigned in register 0x0bh

VLAN Priority Map Register

VLAN_PMR	Offset	Reset Value
VLAN Priority Map Register	$0E_H$	5500_H



Field	Bits	Type	Description
V7	15:14	rw	**Mapped Priority of Tag Value (VLAN) 7** 01_B , default
V6	13:12	rw	**Mapped Priority of Tag Value (VLAN) 6** 01_B , default
V5	11:10	rw	**Mapped Priority of Tag Value (VLAN) 5** 01_B , default
V4	9:8	rw	**Mapped Priority of Tag Value (VLAN) 4** 01_B , default
V3	7:6	rw	**Mapped Priority of Tag Value (VLAN) 3** 00_B , default
V2	5:4	rw	**Mapped Priority of Tag Value (VLAN) 2** 00_B , default
V1	3:2	rw	**Mapped Priority of Tag Value (VLAN) 1** 00_B , default
V0	1:0	rw	**Mapped Priority of Tag Value (VLAN) 0** 00_B , default

00: low priority queue. Q0

01: high priority queue. Q1

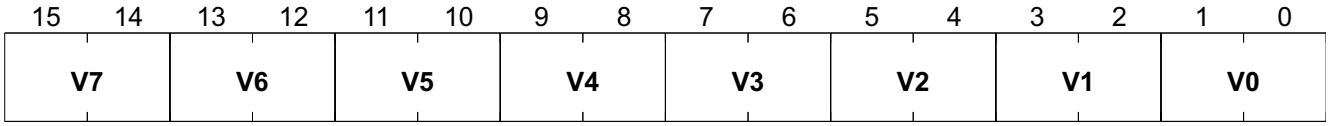
The weight ratio is 1:N. Queue ratio (defined in 0x10h bit[13:12])

Reg. 0x10 Bit[13:12]	Weight Ratio
00	1:1
01	1:2
10	1:3
11	1:4

The default is port-base priority for un-tag packet and none IP frame.

TOS Priority Map Register

TOS_PMR	Offset	Reset Value
TOS Priority Map Register	$0F_H$	5500_H



Field	Bits	Type	Description
V7	15:14	rw	**Mapped Priority of Tag Value (TOS) 7** 01_B , default
V6	13:12	rw	**Mapped Priority of Tag Value (TOS) 6** 01_B , default
V5	11:10	rw	**Mapped Priority of Tag Value (TOS) 5** 01_B , default
V4	9:8	rw	**Mapped Priority of Tag Value (TOS) 4** 01_B , default
V3	7:6	rw	**Mapped Priority of Tag Value (TOS) 3** 00_B , default
V2	5:4	rw	**Mapped Priority of Tag Value (TOS) 2** 00_B , default
V1	3:2	rw	**Mapped Priority of Tag Value (TOS) 1** 00_B , default
V0	1:0	rw	**Mapped Priority of Tag Value (TOS) 0** 00_B , default

00: low priority queue. Q0

01: high priority queue. Q1

The weight ratio is 1:N. Queue ratio (defined in 0x10h/bit[13:12])

Reg. 0x10 Bit[13:12]	Weight Ratio
00	1:1
01	1:2
10	1:3
11	1:4

The default is port-base priority for un-tag packet and none IP frame.

Packet with Priority

- Normal Packet Content

Ethernet Packet from Layer 2

Preamble/SFD	Destination (6 bytes)	Source (6 bytes)	Packet length (2 bytes)	Data (46-1500 bytes)	CRC (4 bytes)
–	Byte 0~5	Byte 6~11	Byte 12~13	Byte 14	–

- VLAN Packet

ADM6999G/GX will check packet byte 12 &13. If byte[12:13] = 8100h then this packet is a VLAN packet.

Tag Protocol TD 8100	Tag Control Information TCI	LEN Length	Routing Information
Byte 12~13	Byte14~15	Byte 16~17	Byte 18

Byte 14~15: Tag Control Information TCI

Bit[15:13]: User Priority 7~0

Bit 12: Canonical Format Indicator (CFI)

Bit[11~0]: VLAN ID. The ADM6999G/GX will use bit[3:0] as VLAN group.

- TOS IP Packet

ADM6999G/GX checks byte 12 &13 if this value is 0800h then ADM6999G/GX knows this is a TOS priority packet.

Type 0800	IP Header
Byte 12~13	Byte 14~15

IP header define

Byte 14

Bit[7:0]: IP protocol version number & header length

Byte 15: Service type

Bit[7~5]: IP Priority (Precedence) from 7~0

Bit 4: No Delay (D)

Bit 3: High Throughput

Bit 2: High Reliability (R)

Bit[1:0]: Reserved

Miscellaneous Configuration Register 0

MCR_0	Offset	Reset Value
Miscellaneous Configuration Register 0	**10_H**	**0040_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res		**QR**		**DM1**		**DM0**		**AD**	Res	Res	**XCRC**	Res	**BSE**	**BST**	

Field	Bits	Type	Description
Res	15:14	ro	**Reserved**
QR	13:12	rw	**Queue Ratio** 00_B , 1:1 01_B , 1:2 10_B , 1:3 11_B , 1:4
DM1	11:10	rw	**Discard Mode (drop scheme for Q1)**
DM0	9:8	rw	**Discard Mode (drop scheme for Q0)**
AD	7	rw	**Aging Disable** 0_B , enable aging, default 1_B , disable aging
Res	6	ro	**Reserved** 0_B , default
Res	5	ro	**Reserved** 0_B , default
XCRC	4	rw	**XCRC Check Disable** 0_B , enable CRC Check, default 1_B , disable CRC check
Res	3	ro	**Reserved** 0_B , default
BSE	2	rw	**Broadcast Storming Enable** 0_B , disable, default 1_B , enable
BST	1:0	rw	**Broadcast Storming Threshold** See below table. 00_B , default

Broadcast storm mode after initial:

Time interval : 50 ms

The max. packet number = 7490 in 100Base, 749 in 10Base

Table 12 Per Port Rising Threshold

	00	01	10	11
All 100TX	Disable	10%	20%	40%
Not All 100TX	Disable	1%	2%	4%

Table 13 Per Port Falling Threshold

	00	01	10	11
All 100TX	Disable	5%	10%	20%
Not All 100TX	Disable	0.5%	1%	2%

Table 14 Drop Scheme for each Queue

Discard Mode/ Utilization	00	01	10	11
TBD	0%	0%	25%	50%

VLAN Mode Select Register

VLAN_MSR	Offset	Reset Value
VLAN Mode Select Register	11_H	$FF00_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					**BP**	**T**	Res	Res		**MS**	**CE**	Res			

Field	Bits	Type	Description
Res	15:11	ro	**Reserved** 11111_B , default
BP	10	rw	**Back-pressure Enable** This is a global pin for all ports. 0_B , disable 1_B , enable, default
T	9	ro	**Reserved** 1_B , default
Res	8	ro	**Reserved** 1_B , default
Res	7:6	ro	**Reserved** 00_B , default
MS	5	rw	**VLAN Mode Select** 0_B , by-pass mode with port-base VLAN, default 1_B , 802.1Q base VLAN
CE	4	rw	**MAC Clone Enable** 0_B , Normal mode. Learning with SA only. ADM6999G/GX fills/searches MAC table by SA or DA only. Default. 1_B , MAC Clone mode. Learning with SA, VID0. ADM6999G/GX fills/searches MAC table by SA or DA with VID0. This bit makes the chip learn two same addresses with different VID0.
Res	3:0	ro	**Reserved** 0000_B , default

Below is Bit4, 5 VLAN Tag and MAC application example base on Infineon-ADMtek Co Ltd ADM6996.

Table 15 ADM6996 Port Mapping with ADM6999G/GX

ADM6996	ADM6999G/GX
Port0	Port0
–	Port1
Port1	Port2
–	Port3

Table 15 ADM6996 Port Mapping with ADM6999G/GX (cont'd)

ADM6996	ADM6999G/GX
Port2	Port4
–	Port5
Port3	Port6
Port4	Port7
Port5 MII	Port8 MII

Below is Router old architecture. The disadvantages of this are:

1. WAN port only supports 10M Half-Duplex and non-MDIX function.
2. Needs extra 10M NIC costs.
3. ISA bus will become bottleneck of whole system.

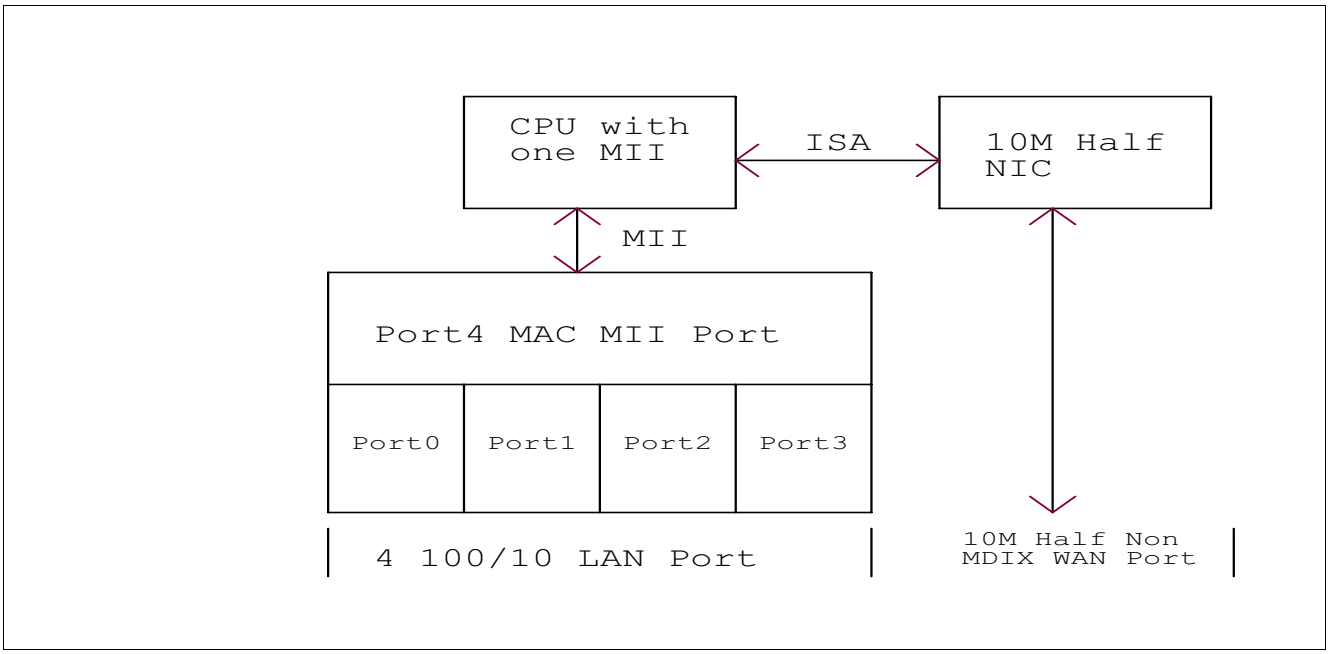


Figure 5 Router old architecture

Below is new architecture by using ADM6996 serial chip VLAN function. The advantages of below are:

1. WAN Port can upgrade to 100/10 Full/Half, Auto MDIX.
2. WAN/LAN Port is programmable and put on same Switch.
3. No extra NIC and save the cost.
4. High bandwidth of MII port up to 200M speed.

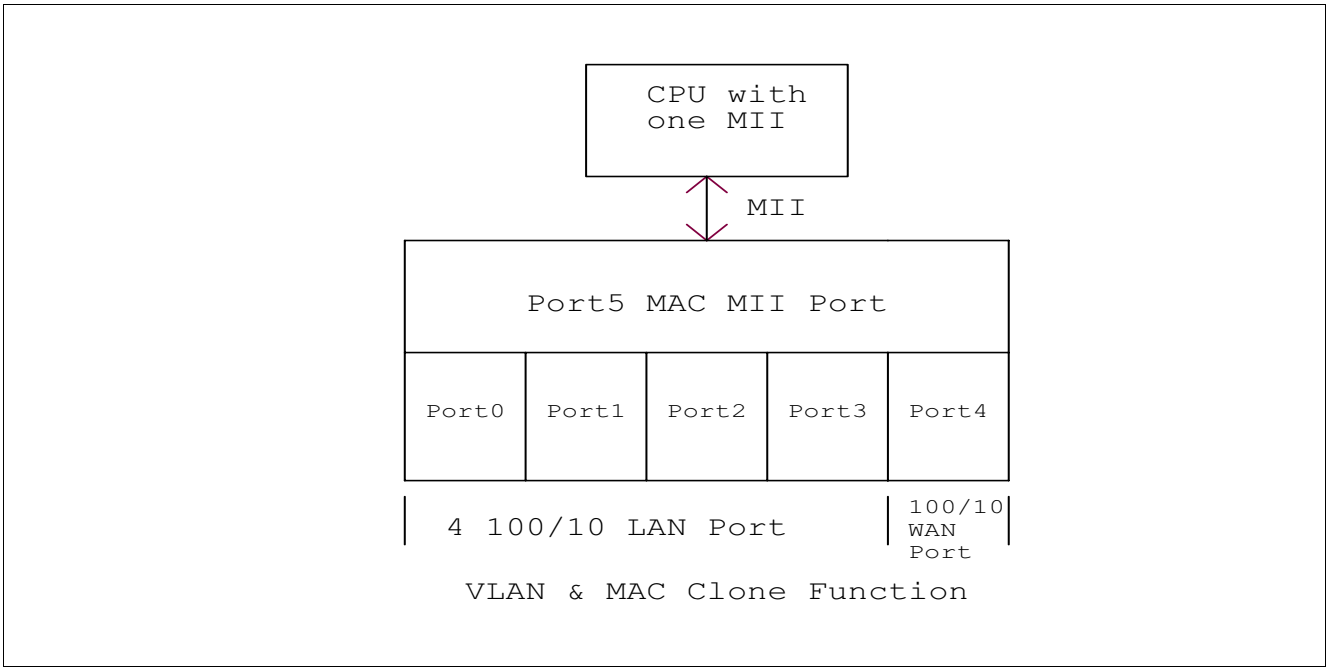


Figure 6 New architecture by using ADM6999G/GX serial chip VLAN function

New Router application works well on the normal application. If user's ISP vendor (cable modem) lock Registration Card's ID then Router CPU must send this Lock Registration Card's ID to WAN Port. One condition that may happen is that there exists two same MAC ID on this Switch. One is the original Card and another one is CPU. This will make Switch learning table have the trouble.

ADM6999G/GX provides MAC Clone function that allows two the same MAC addresses with different VLAN ID0 on learning table. This will solve Lock registration Card's ID issue. ADM6999G/GX serial chip will put these two same MAC addresses with different VLAN ID0 at different learning table's entry.

How to Set ADM6999G/GX on Router:

- Port0~3: LAN Port
- Port4: WAN Port
- Port5: MII Port as CPU Port

Step1: Set Register 11_H bit4 and bit5 to 1.

{Coding: Write Register 11_H as 0xff30h}

Step2: Set Port0~3 as Untag Port and set PVID = 1.

{Coding: Write Register 01_H, 03_H, 05_H, 07_H as $840F_H$. Port0~3 as Untag, PVID = 1, Enable MDIX}

Step3: Set Port4 as Untag Port and set PVID = 2.

{Coding: Write Register 08_H as $880F_H$. Port4 as Untag, PVID = 2, Enable MDIX.}

Step4: Set Port5 MII Port as Tag Port and set PVID = 2.

{Coding: Write Register 09_H as $881F_H$. Port5 MII port as Tag, PVID = 2.}

Step5: Group Port0, 1, 2, 3, 5 as VLAN 1.

{Coding: Write Register 14_H as 0155_H. VLAN1 cover Port0, 1, 2, 3, 5.}

Step6: Group Port4, 5 as VLAN 2.

{Coding: Write Register 15_H as 0180_H. VLAN2 cover Port4, 5.}

How MAC Clone Operation:

1. LAN to LAN/CPU Traffic. ADM6999G/GX LAN traffic to LAN/CPU only. Traffic to another LAN port will be untagged packet. Traffic to CPU is Tagged packet with VID = 1. CPU can check VID to distinguish LAN traffic or WAN traffic.
2. WAN to CPU Traffic. ADM6999G/GX WAN traffic to CPU only. Traffic to CPU is Tagged packet with VID = 2. CPU can check VID to distinguish LAN traffic or WAN traffic.
3. CPU to LAN Packet. ADM6999G/GX CPU Packet to LAN port must add VID = 1 in VLAN field. ADM6999G/GX check VID to distinguish LAN traffic or WAN traffic. LAN output packet is Untagged.
4. CPU to WAN Packet. ADM6999G/GX CPU Packet to WAN port must add VID = 2 in VLAN filed. ADM6999G/GX check VID to distinguish LAN traffic or WAN traffic. WAN output packet is Untagged.
5. ADM6999G/GX learning sequence. ADM6999G/GX will check VLAN mapping setting first then check learning table. Users don't have to worry about LAN/WAN traffic mixing up.

Note: Bit 10: Half Duplex Back Pressure enable. 1/enable, 0/disable.

Miscellaneous Configuration Register 2

MCR_2	Offset	Reset Value
Miscellaneous Configuration Register 2	**12_H**	**3600_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DP	Res	**PS**		Res	Res		**ML8**	**ML7**	**ML6**	**ML5**	**ML4**	**ML3**	**ML2**	**ML1**	**ML0**

Field	Bits	Type	Description
DP	15	rw	**Drop Packet when Excessive Collision Happen Enable** 0_B , Disable, default 1_B , enable
Res	14	ro	**Reserved**
PS	13:12	rw	**Power Saving Select**
Res	11:9	ro	**Reserved**
ML8	8	rw	**Port8 MAC Lock.** 0_B , Disable, default 1_B , Lock first MAC source address
ML7	7	rw	**Port7 MAC Lock** 0_B , Disable, default 1_B , Lock first MAC source address
ML6	6	rw	**Port6 MAC Lock** 0_B , Disable, default 1_B , Lock first MAC source address
ML5	5	rw	**Port5 MAC Lock** 0_B , Disable, default 1_B , Lock first MAC source address
ML4	4	rw	**Port4 MAC Lock** 0_B , Disable, default 1_B , Lock first MAC source address

Field	Bits	Type	Description
ML3	3	rw	**Port3 MAC Lock** 0_B , Disable, default 1_B , Lock first MAC source address
ML2	2	rw	**Port2 MAC Lock** 0_B , Disable, default 1_B , Lock first MAC source address
ML1	1	rw	**Port1 MAC Lock** 0_B , Disable, default 1_B , Lock first MAC source address
ML0	0	rw	**Port0 MAC Lock** 0_B , Disable, default 1_B , Lock first MAC source address

Notes

1. *Bit [8:0]: Port Locking enable. Learn one MAC ID when enable. 1/enable. 0/disable.*
2. *Bit[15]: Half Duplex excessive collision (16) drop packet enable. 1/drop. 0/no drop.*

VLAN Mapping Table Register 0

16 VLAN Group: See Register $2C_H$ bit 11_B = 0

VLAN_MTR_0	Offset	Reset Value
VLAN Mapping Table Register 0	13_H	$FFFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res							P8	P7	P6	P5	P4	P3	P2	P1	P0

Field	Bits	Type	Description
P8	8	rw	**VLAN Mapping Table** Port8
P7	7	rw	**VLAN Mapping Table** Port7
P6	6	rw	**VLAN Mapping Table** Port6
P5	5	rw	**VLAN Mapping Table** Port5
P4	4	rw	**VLAN Mapping Table** Port4
P3	3	rw	**VLAN Mapping Table** Port3
P2	2	rw	**VLAN Mapping Table** Port2

Field	Bits	Type	Description
P1	1	rw	**VLAN Mapping Table** Port1
P0	0	rw	**VLAN Mapping Table** Port0

Select VLAN group's port is to set the corresponding bit to 1.

VLAN Mapping Table Registers 0

32 VLAN Group: See Register $2C_H$ bit 11_B = 1

VLAN_MTR	**Offset**	**Reset Value**
VLAN Mapping Table Registers	**13_H**	**$FFFF_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P7	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**	**P7**	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**

Field	Bits	Type	Description
P7	15	rw	**Port 7, Odd VLAN Mapping Table**
P6	14	rw	**Port 6, Even VLAN Mapping Table**
P5	13	rw	**Port 5, Odd VLAN Mapping Table**
P4	12	rw	**Port 4, Even VLAN Mapping Table**
P3	11	rw	**Port 3, Odd VLAN Mapping Table**
P2	10	rw	**Port 2, Even VLAN Mapping Table**
P1	9	rw	**Port 1, Odd VLAN Mapping Table**
P0	8	rw	**Port 0, Even VLAN Mapping Table**
P7	7	rw	**Port 7, Odd VLAN Mapping Table**
P6	6	rw	**Port 6, Even VLAN Mapping Table**
P5	5	rw	**Port 5, Odd VLAN Mapping Table**
P4	4	rw	**Port 4, Even VLAN Mapping Table**
P3	3	rw	**Port 3, Odd VLAN Mapping Table**
P2	2	rw	**Port 2, Even VLAN Mapping Table**
P1	1	rw	**Port 1, Odd VLAN Mapping Table**
P0	0	rw	**Port 0, Even VLAN Mapping Table**

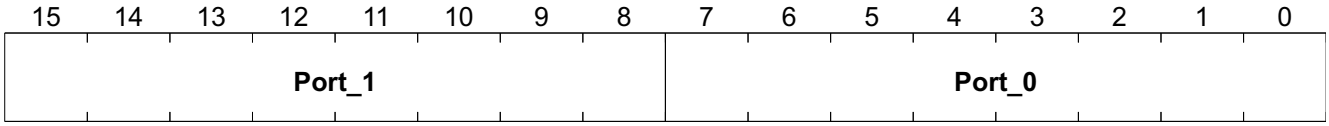
All VLAN groups will cover Port8 at 32 group mode. This feature is good for multiple ADM6999G/GX systems.

Table 16 VLAN_MTR_x Registers Table

Register Short Name	Register Long Name	Offset Address	Page Number
VLAN_MTR_1	VLAN Mapping Table Register 1	14_H	
VLAN_MTR_2	VLAN Mapping Table Register 2	15_H	
VLAN_MTR_3	VLAN Mapping Table Register 3	16_H	
VLAN_MTR_4	VLAN Mapping Table Register 4	17_H	
VLAN_MTR_5	VLAN Mapping Table Register 5	18_H	
VLAN_MTR_6	VLAN Mapping Table Register 6	19_H	
VLAN_MTR_7	VLAN Mapping Table Register 7	$1A_H$	
VLAN_MTR_8	VLAN Mapping Table Register 8	$1B_H$	
VLAN_MTR_9	VLAN Mapping Table Register 9	$1C_H$	
VLAN_MTR_10	VLAN Mapping Table Register 10	$1D_H$	
VLAN_MTR_11	VLAN Mapping Table Register 11	$1E_H$	
VLAN_MTR_12	VLAN Mapping Table Register 12	$1F_H$	
VLAN_MTR_13	VLAN Mapping Table Register 13	20_H	
VLAN_MTR_14	VLAN Mapping Table Register 14	21_H	
VLAN_MTR_15	VLAN Mapping Table Register 15	22_H	

Port Buffer Threshold Control Registers P0, P1

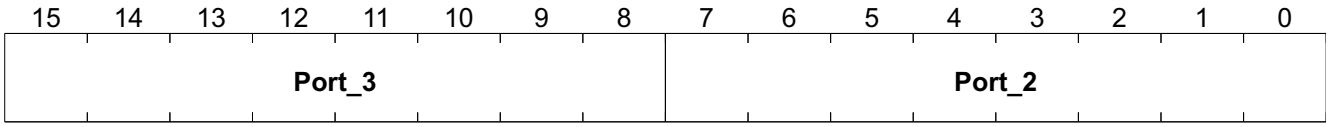
PBTCR_P01	Offset	Reset Value
Port Buffer Threshold Control Reg. P0, P1	23_H	0000_H



Field	Bits	Type	Description
Port_1	15:8	rw	**Port1, Odd Port Buffer Threshold Control**
Port_0	7:0	rw	**Port0, Even Port Buffer Threshold Control**

Port Buffer Threshold Control Register P2, P3

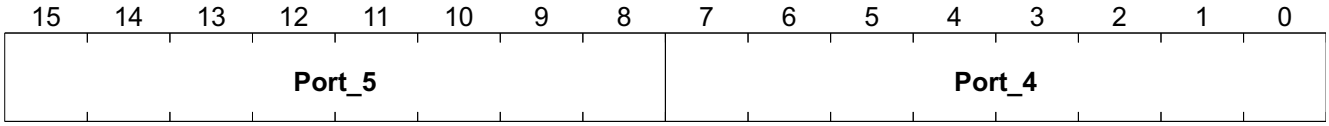
PBTCR_P23	Offset	Reset Value
Port Buffer Threshold Control Reg. P2, P3	24_H	0000_H



Field	Bits	Type	Description
Port_3	15:8	rw	**Port3, Odd Port Buffer Threshold Control**
Port_2	7:0	rw	**Port2, Even Port Buffer Threshold Control**

Port Buffer Threshold Control Register P4, P5

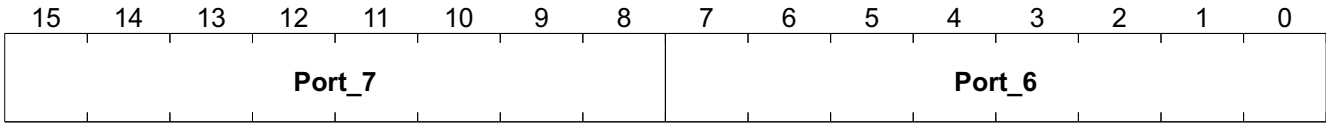
PBTCR_P45	Offset	Reset Value
Port Buffer Threshold Control Reg. P4, P5	25_H	0000_H



Field	Bits	Type	Description
Port_5	15:8	rw	**Port5, Odd Port Buffer Threshold Control**
Port_4	7:0	rw	**Port4, Even Port Buffer Threshold Control**

Port Buffer Threshold Control Register P6, P7

PBTCR_P67	Offset	Reset Value
Port Buffer Threshold Control Reg. P6, P7	26_H	0000_H



Field	Bits	Type	Description
Port_7	15:8	rw	**Port7, Odd Port Buffer Threshold Control**
Port_6	7:0	rw	**Port6, Even Port Buffer Threshold Control**

ADM6999G/GX supports buffer management scheme with dynamic thresholds to ensure the fair share of memory among different port queues. If users need each port to have a fixed threshold, they can configure the Bit 14 in the 27_H to 1.

Dynamic threshold management:

Bit[7]: The add bit. Bit[6:0]: The offset bits.

When Bit[7] = 1, the switch will use the value (buffers really used + 2*bit[6:0]) as the buffer count that the port has used.

When Bit[7] = 0, the switch will use the value (buffers really used - 2*bit[6:0]) as the buffer count that the port has used.

Fixed threshold management:

Bit[3:0]: The buffer threshold bits.

When the total buffer was not reached, the buffer amount allocated to each port will be equal to bit[3:0] * 4.

Total Buffer Threshold Control Register

TBTCR	Offset	Reset Value
Total Buffer Threshold Control Register	**27_H**	**0000_H**

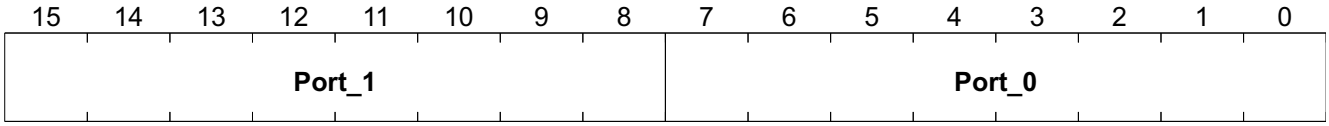
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	Res	**TBTC**						**PBTC**							

Field	Bits	Type	Description
Res	15	ro	**Reserved** 0_B , default
Res	14	ro	**Reserved** 0_B , default
TBTC	13:8	rw	**Total Buffer Threshold Control**
PBTC	7:0	rw	**Port8 Buffer Threshold Control** The configuration is same as the other ports.

Dynamic threshold management: Bit[13]: The add bit. Bit[12:8]: The offset bits.When Bit[13] = 1, the switch will use the value (buffers really used + 8*bit[12:8]) as the buffer count that the switch has used.When Bit[13] = 0, the switch will use the value (buffers really used - 8*bit[12:8]) as the buffer count that the switch has used.Fixed threshold management:Bit[13]: This bit doesn't affect the threshold.Bit[12:8]: The total buffer threshold bits.

Port0, 1 PVID bit11~4 Configuration Register

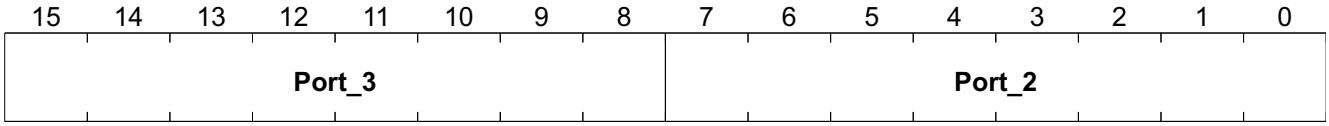
PVID11_4_CR_P01	Offset	Reset Value
Port0, 1 PVID bit11~4 Configuration Register	28_H	0000_H



Field	Bits	Type	Description
Port_1	15:8	rw	**Port1 PVID bit 11~4** These 8 bits combine with register 02_H Bit[13~10] as full 12 bit VID. 00_H , default
Port_0	7:0	rw	**Port0 PVID bit 11~4** These 8 bits combine with register 01_H Bit[13~10] as full 12 bit VID. 00_H , default

Port2, 3 PVID bit11~4 Configuration Register

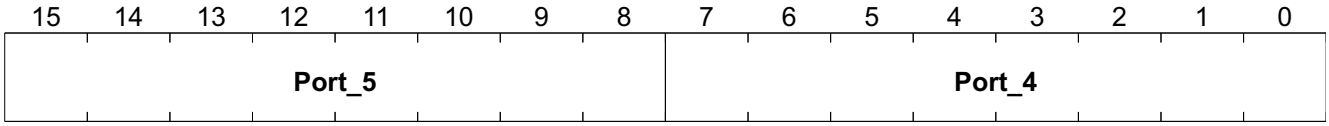
PVID11_4_CR_P23	Offset	Reset Value
Port2, 3 PVID bit11~4 Configuration Register	29_H	0000_H



Field	Bits	Type	Description
Port_3	15:8	rw	**Port3 PVID bit 11~4** These 8 bits combine with register 04_H Bit[13~10] as full 12 bit VID. 00_H , default
Port_2	7:0	rw	**Port2 PVID bit 11~4** These 8 bits combine with register 03_H Bit[13~10] as full 12 bit VID. 00_H , default

Port4, 5 PVID bit 11~4 Configuration Register

PVID11_4_CR_P45	Offset	Reset Value
Port4, 5 PVID bit 11~4 Configuration Register	$2A_H$	0000_H

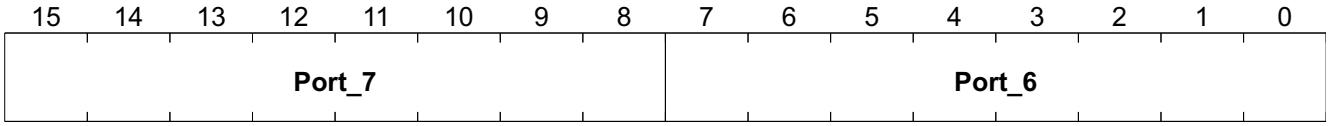


Field	Bits	Type	Description
Port_5	15:8	rw	**Port5 PVID bit 11~4** These 8 bits combine with register 06_H Bit[13~10] as full 12 bit VID. 00_H , default
Port_4	7:0	rw	**Port4 PVID bit 11~4** These 8 bits combine with register 05_H Bit[13~10] as full 12 bit VID. 00_H , default

Port6, 7 PVID bit 11~4 Configuration Register

PVID11_4_CR_P67 — **Offset** — **Reset Value**

Port6, 7 PVID bit 11~4 Configuration Register — **$2B_H$** — **0000_H**

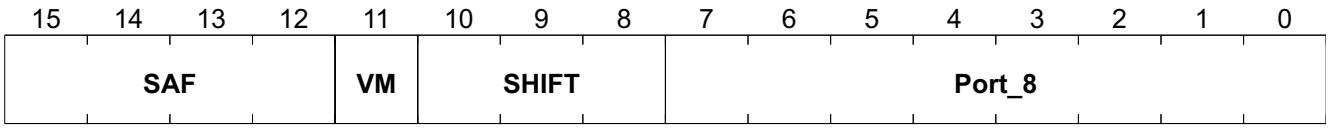


Field	Bits	Type	Description
Port_7	15:8	rw	**Port7 PVID bit 11~4** These 8 bits combine with register 08_H Bit[13~10] as full 12 bit VID. 00_H , default
Port_6	7:0	rw	**Port6 PVID bit 11~4** These 8 bits combine with register 07_H Bit[13~10] as full 12 bit VID. 00_H , default

Port8 PVID bit 11~4 and VLAN Group Shift Bits Configuration Register

PVID11_4_VLAN_CR — **Offset** — **Reset Value**

P8 PVID bit 11~4/VLAN Group Shift Bits Conf. — **$2C_H$** — **$D000_H$**



Field	Bits	Type	Description
SAF	15:12	rw	**Special Address Forwarding** IEEE 802.3 reserved DA forward or drop police 1101_H , default **Bit[15]** Control reserved MAC (0180C2000010-0180C20000FF) 0_B , Discard 1_B , Forward, default **Bit[14]** Control reserved MAC (0180C2000002- 0180C200000F) 0_B , Discard 1_B , Forward, default **Bit[13]** Control reserved MAC (0180C2000001) 0_B , Discard, default 1_B , Forward **Bit[12]** Control reserved MAC (0180C2000000) 0_B , Discard 1_B , Forward, default
VM	11	rw	**VLAN Mode** Select 16 or 32 VLAN group. 0_B , 16 VLAN group,default 1_B , 32 VLAN group,default
SHIFT	10:8	rw	**Tag Shift for VLAN Grouping** VLAN Tagshift register. ADM6999G/GX will select 4/5 bit from total 12 bit VID as VLAN groupreference. Select 4 or 5 bits from VID depends on bit 11 setting. For example Bit[10:8] = 001, Bit11 = 0,then ADM6999G/GX will select packet VID4~VID1 as VLAN group mapping. It is very flexible for user on VLAN grouping. $00C_H$, default **16 VLAN Mode** 0_D , VID[3:0] 1_D , VID[4:1] 2_D , VID[5:2] 3_D , VID[6:3] 4_D , VID[7:4] 5_D , VID[8:5] 6_D , VID[9:6] 7_D , VID[10:7] **32 VLAN Mode** 0_D , VID[4:0] 1_D , VID[5:1] 2_D , VID[6:2] 3_D , VID[7:3] 4_D , VID[8:4] 5_D , VID[9:5] 6_D , VID[10:6] 7_D , VID[11:7]

Field	Bits	Type	Description
Port_8	7:0	rw	**Expansion Port PVID bit 11~4** These 8 bits combine with register 09_H Bit[13~10] as full 12 bit VID. 00_H , default

3.6 EEPROM Access Description

Customers can select ADM6999G/GX read EEPROM contents as chip setting or not. ADM6999G/GX will check the signature of EEPROM to decide read content of EEPROM or not.

Table 17 RC & EEPROM Content Relationship

RC	CS	SK	DI	DO
0	High Impedance	High Impedance	High Impedance	High Impedance
Rising edge 01 (30ms)	Output	Output	Output	Input
1 (after 30 ms)	Input	Input	I/O	Input

Keep at least 30 ms after RC from 0 to 1. ADM6999G/GX will read data from EEPROM. After RC from 0 to 1, if CPU update EEPROM then ADM6999G/GX will update configuration registers too.

When CPU programs EEPROM & ADM6999G/GX, ADM6999G/GX recognizes the EEPROM WRITE instruction only. If there is any Protection instruction before or after the EEPROM WRITE instruction, CPU needs to generate separated CS signal cycle for each Protection & WRITE instruction.

CPU can directly program ADM6999G/GX after 30ms of Reset signal rising edge with or without EEPROM.

ADM6999G/GX serial chips will latch hardware-reset value as recommend value. It includes EEPROM interface:

- EECS: Internal Pull down 40K resister
- EESK: TP port Auto-MDIX select. Internal pull down 40K resister as non Auto-MDIX mode.
- EDI: Dual Color Select. Internal pull down 40K resister as Single Color Mode.
- EDO: EEPROM enable. Internal pull up 40K resister as EEPROM enable.

Below Figure is ADM6999G/GX serial chips EEPROM pins operation at different stages. Reset signal is controlled by CPU with at least 100ms low. Point1 is Reset rising edge. CPU must prepare proper value on ECS(0), EESK, EDI, EDO(1) before this rising edge. ADM6999G/GX will read this value into chip at Point2. CPU must keep these values over point2. Point2 is 200ns after Reset rising edge.

ADM6999G/GX serial chips will read EEPROM content at Point4 which 800ns far away from the rising edge of Reset. CPU must turn EEPROM pins EECS, EESK, EDI and EDO to High-Z or pull high before Point4.

If users want to change the state to High-Z or pull high on EEPROM pins, the order is CS-> DI -> DO -> SK is better.

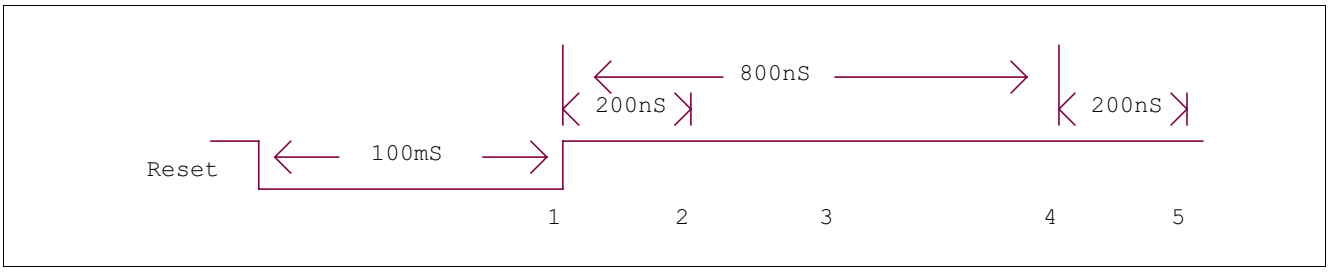


Figure 7 ADM6999G/GX serial chips EEPROM pins operation

The timing for writing to EEPROM is a little bit different. See below graph. Must be carefull when CS goes down after writting a command, SK must issue at least one clock. This is a difference between ADM6999G/GX with EEPROM write timing. If the system is without EEPROM then users must write ADM6999G/GX internal register by 93C66 timing. If users use EEPROM then the writing timing depends on EEPROM type.

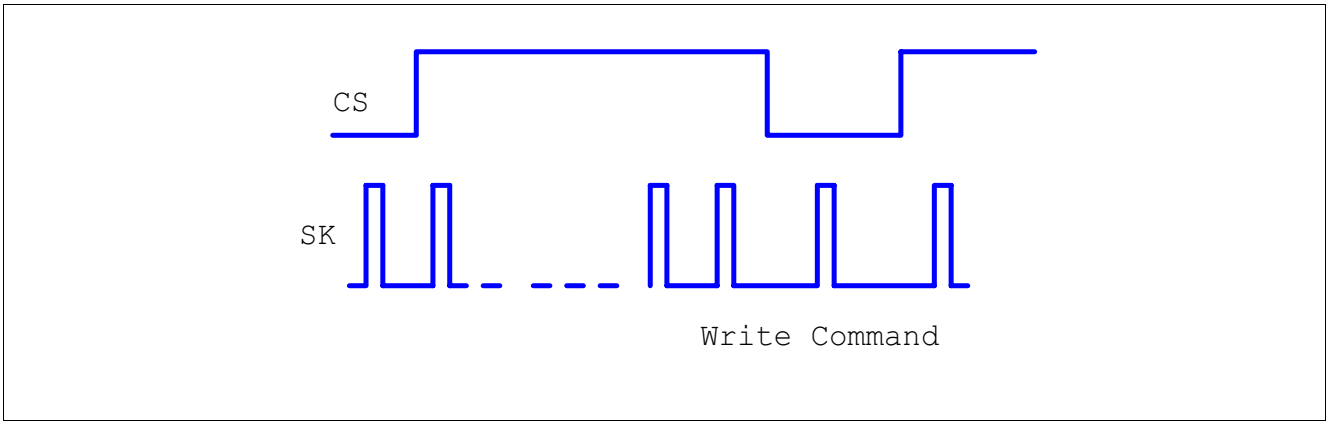


Figure 8 EEPROM Writing Command

4 Serial Management

4.1 Serial Registers Map

Table 18 Registers Address SpaceRegisters Address Space

Module	Base Address	End Address	Note
Serial	00_H	$3C_H$	

Table 19 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
Chip_ID	Chip Identifier Register	00_H	65
PSR_0	Port Status 0 Register	01_H	66
PSR_1	Port Status 1 Register	02_H	69
CBSR	Cable Broken Status Register	03_H	70
RPC_0	Port 0 Receive Packet Count	04_H	70
RPC_1	Port 1 Receive Packet Count	05_H	71
RPBC_2	Port 2 Receive Packet Byte Count	05_H	71
RPC_2	Port 2 Receive Packet Count	06_H	71
RPC_3	Port 3 Receive Packet Count	07_H	71
RPC_4	Port 4 Receive Packet Count	08_H	71
RPC_5	Port 5 Receive Packet Count	09_H	71
RPC_6	Port 6 Receive Packet Count	$0A_H$	71
RPC_7	Port 7 Receive Packet Count	$0B_H$	71
RPC_8	Port 8 Receive Packet Count	$0C_H$	71
RPBC_0	Port 0 Receive Packet Byte Count	$0E_H$	71
RPBC_1	Port 1 Receive Packet Byte Count	$0F_H$	71
RPBC_3	Port 3 Receive Packet Byte Count	10_H	71
RPBC_4	Port 4 Receive Packet Byte Count	11_H	71
RPBC_5	Port 5 Receive Packet Byte Count	12_H	71
RPBC_6	Port 6 Receive Packet Byte Count	13_H	71
RPBC_7	Port 7 Receive Packet Byte Count	14_H	71
RPBC_8	Port 8 Receive Packet Byte Count	15_H	71
TPC_0	Port 0 Transmit Packet Count	16_H	71
TPC_1	Port 1 Transmit Packet Count	17_H	71
TPC_2	Port 2 Transmit Packet Count	18_H	71
TPC_3	Port 3 Transmit Packet Count	19_H	71
TPC_4	Port 4 Transmit Packet Count	$1A_H$	71
TPC_5	Port 5 Transmit Packet Count	$1B_H$	71
TPC_6	Port 6 Transmit Packet Count	$1C_H$	71
TPC_7	Port 7 Transmit Packet Count	$1D_H$	71

Table 19 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
TPC_8	Port 8 Transmit Packet Count	$1E_H$	71
TPBC_0	Port 0 Transmit Packet Byte Count	$1F_H$	71
TPBC_1	Port 1 Transmit Packet Byte Count	20_H	71
TPBC_2	Port 2 Transmit Packet Byte Count	21_H	71
TPBC_3	Port 3 Transmit Packet Byte Count	22_H	71
TPBC_4	Port 4 Transmit Packet Byte Count	23_H	71
TPBC_5	Port 5 Transmit Packet Byte Count	24_H	71
TPBC_6	Port 6 Transmit Packet Byte Count	25_H	71
TPBC_7	Port 7 Transmit Packet Byte Count	26_H	71
TPBC_8	Port 8 Transmit Packet Byte Count	27_H	72
CC_0	Port 0 Collision Count	28_H	72
CC_1	Port 1 Collision Count	29_H	72
CC_2	Port 2 Collision Count	$2A_H$	72
CC_3	Port 3 Collision Count	$2B_H$	72
CC_4	Port 4 Collision Count	$2C_H$	72
CC_5	Port 5 Collision Count	$2D_H$	72
CC_6	Port 6 Collision Count	$2E_H$	72
CC_7	Port 7 Collision Count	$2F_H$	72
CC_8	Port 8 Collision Count	30_H	72
EC_0	Port 0 Error Count	31_H	72
EC_1	Port 1 Error Count	32_H	72
EC_2	Port 2 Error Count	33_H	72
EC_3	Port 3 Error Count	34_H	72
EC_4	Port 4 Error Count	35_H	72
EC_5	Port 5 Error Count	36_H	72
EC_6	Port 6 Error Count	37_H	72
EC_7	Port 7 Error Count	38_H	72
EC_8	Port 8 Error Count	39_H	72
OFFR_0	Over Flow Flag 0 Register	$3A_H$	73
OFFR_1	Over Flow Flag 1 Register	$3B_H$	74
OFFR_2	Over Flow Flag 2 Register	$3C_H$	75

The register is addressed wordwise.

Table 20 Register Access Types

Mode	Symbol	Description HW	Description SW
read/write	rw	Register is used as input for the HW	Register is readable and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)

Table 20 Register Access Types (cont'd)

Mode	Symbol	Description HW	Description SW
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latches high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latches high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latches high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latches high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiates the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiates the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiates the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiates the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is readable and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is readable and writable by SW.

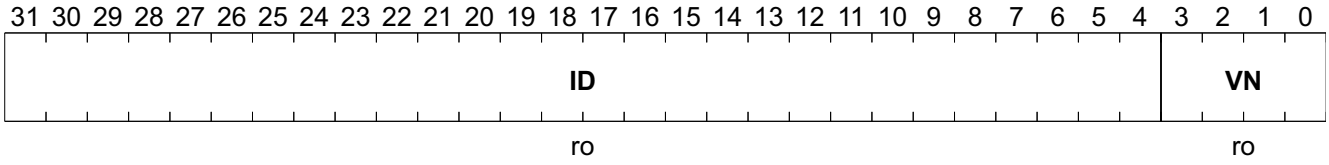
Table 21 Registers Clock DomainsRegisters Clock Domains

Clock Short Name	Description

4.1.1 Serial Registers Description

Chip Identifier Register

Chip_ID	Offset	Reset Value
Chip Identifier Register	**00_H**	**$0002\ 1120_H$**

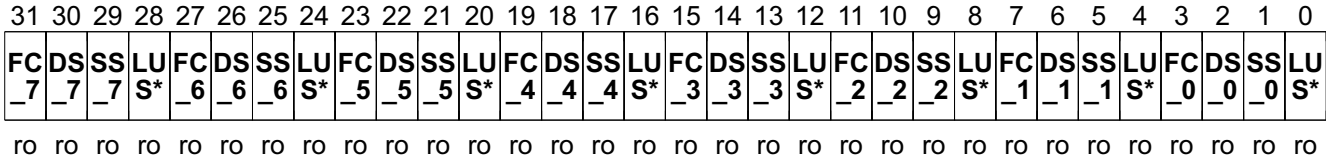


Field	Bits	Type	Description
ID	31:4	ro	**ID** 0002112_H **ID**,
VN	3:0	ro	**Version number** 0000_B **VN**,

Port Status 0 Register

PSR_0 **Offset** **Reset Value**

Port Status 0 Register **01_H** **$0000\ 0000_H$**



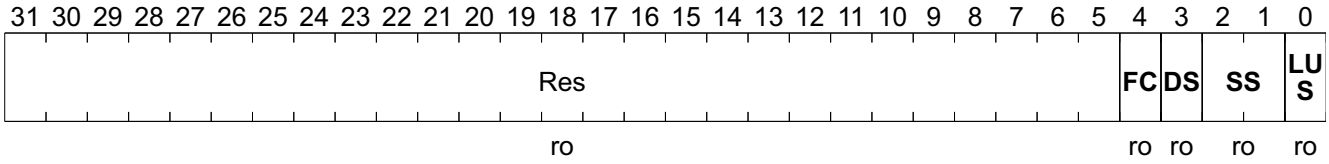
Field	Bits	Type	Description
FC_7	31	ro	**Port 7 Flow Control Enable** 0_B , Flow Control Disable 1_B , 802.3X on for full duplex or back pressure on for half duplex
DS_7	30	ro	**Port 7 Duplex Status** 0_B , Half Duplex 1_B , Full Duplex
SS_7	29	ro	**Port 7 Speed Status** 0_B , 10 Mbit/s 1_B , 100 Mbit/s
LUS_7	28	ro	**Port 7 Linkup Status** 0_B , Link is not established 1_B , Link is established
FC_6	27	ro	**Port 6 Flow Control Enable** 0_B , Flow Control Disable 1_B , 802.3X on for full duplex or back pressure on for half duplex
DS_6	26	ro	**Port 6 Duplex Status** 0_B , Half Duplex 1_B , Full Duplex
SS_6	5	ro	**Port 6 Speed Status** 0_B , 10 Mbit/s 1_B , 100 Mbit/s

Field	Bits	Type	Description
LUS_6	24	ro	**Port 6 Linkup Status** 0_B , Link is not established 1_B , Link is established
FC_5	23	ro	**Port 5 Flow Control Enable** 0_B , Flow Control Disable 1_B , 802.3X on for full duplex or back pressure on for half duplex
DS_5	22	ro	**Port 5 Duplex Status** 0_B , Half Duplex 1_B , Full Duplex
SS_5	21	ro	**Port 5 Speed Status** 0_B , 10 Mbit/s 1_B , 100 Mbit/s
LUS_5	20	ro	**Port 5 Linkup Status** 0_B , Link is not established 1_B , Link is established
FC_4	19	ro	**Port 4 Flow Control Enable** 0_B , Flow Control Disable 1_B , 802.3X on for full duplex or back pressure on for half duplex
DS_4	18	ro	**Port 4 Duplex Status** 0_B , Half Duplex 1_B , Full Duplex
SS_4	17	ro	**Port 4 Speed Status** 0_B , 10 Mbit/s 1_B , 100 Mbit/s
LUS_4	16	ro	**Port 4 Linkup Status** 0_B , Link is not established 1_B , Link is established
FC_3	15	ro	**Port 3 Flow Control Enable** 0_B , Flow Control Disable 1_B , 802.3X on for full duplex or back pressure on for half duplex
DS_3	14	ro	**Port 3 Duplex Status** 0_B , Half Duplex 1_B , Full Duplex
SS_3	13	ro	**Port 3 Speed Status** 0_B , 10 Mbit/s 1_B , 100 Mbit/s
LUS_3	12	ro	**Port 3 Linkup Status** 0_B , Link is not established 1_B , Link is established
FC_2	11	ro	**Port 2 Flow Control Enable** 0_B , Flow Control Disable 1_B , 802.3X on for full duplex or back pressure on for half duplex
DS_2	10	ro	**Port 2 Duplex Status** 0_B , Half Duplex 1_B , Full Duplex

Field	Bits	Type	Description
SS_2	9	ro	**Port 2 Speed Status** 0_B , 10 Mbit/s 1_B , 100 Mbit/s
LUS_2	8	ro	**Port 2 Linkup Status** 0_B , Link is not established 1_B , Link is established
FC_1	7	ro	**Port 1 Flow Control Enable** 0_B , Flow Control Disable 1_B , 802.3X on for full duplex or back pressure on for half duplex
DS_1	6	ro	**Port 1 Duplex Status** 0_B , Half Duplex 1_B , Full Duplex
SS_1	5	ro	**Port 1 Speed Status** 0_B , 10 Mbit/s 1_B , 100 Mbit/s
LUS_1	4	ro	**Port 1 Linkup Status** 0_B , Link is not established 1_B , Link is established
FC_0	3	ro	**Port 0 Flow Control Enable** 0_B , Flow Control Disable 1_B , 802.3X on for full duplex or back pressure on for half duplex
DS_0	2	ro	**Port 0 Duplex Status** 0_B , Half Duplex 1_B , Full Duplex
SS_0	1	ro	**Port 0 Speed Status** 0_B , 10 Mbit/s 1_B , 100 Mbit/s
LUS_0	0	ro	**Port 0 Linkup Status** 0_B , Link is not established 1_B , Link is established

Port Status 1 Register

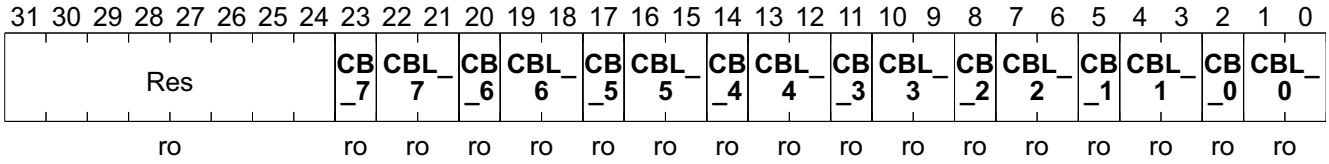
PSR_1	Offset	Reset Value
Port Status 1 Register	02_H	$0000\ 0000_H$



Field	Bits	Type	Description
Res	31:5	ro	**Reserved** 0_H , default
FC	4	ro	**Port 8 Flow Control Enable** 0_B , Flow Control Disable 1_B , 802.3X on for full duplex or back pressure on for half duplex
DS	3	ro	**Port 8 Duplex Status** 0_B , Half Duplex 1_B , Full Duplex
SS	2:1	ro	**Port 8 Speed Status** Two bits indicate the operating speed 00_B , 10 Mbit/s 01_B , 100 Mbit/s $1x_B$, 1000 Mbit/s
LUS	0	ro	**Port 8 Linkup Status** 0_B , Link is not established 1_B , Link is established

Cable Broken Status Register

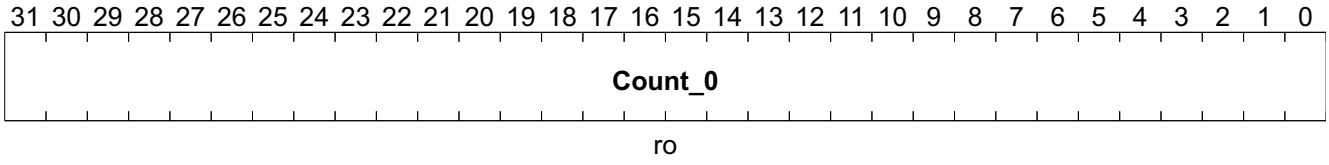
CBSR	Offset	Reset Value
Cable Broken Status Register	03_H	$0000\ 0000_H$



Field	Bits	Type	Description
Res	31:24	ro	**Reserved** 0_H , default
CB_7	23	ro	**Port 7 Cable Broken**
CBL_7	22:21	ro	**Port 7 Cable Broken Length**
CB_6	20	ro	**Port 6 Cable Broken**
CBL_6	19:18	ro	**Port 6 Cable Broken Length**
CB_5	17	ro	**Port 5 Cable Broken**
CBL_5	16:15	ro	**Port 5 Cable Broken Length**
CB_4	14	ro	**Port 4 Cable Broken**
CBL_4	13:12	ro	**Port 4 Cable Broken Length**
CB_3	11	ro	**Port 3 Cable Broken**
CBL_3	10:9	ro	**Port 3 Cable Broken Length**
CB_2	8	ro	**Port 2 Cable Broken**
CBL_2	7:6	ro	**Port 2 Cable Broken Length**
CB_1	5	ro	**Port 1 Cable Broken**
CBL_1	4:3	ro	**Port 1 Cable Broken Length**
CB_0	2	ro	**Port 0 Cable Broken**
CBL_0	1:0	ro	**Port 0 Cable Broken Length**

Port 0 Receive Packet Count

RPC_0	Offset	Reset Value
Port 0 Receive Packet Count	04_H	$0000\ 0000_H$



Field	Bits	Type	Description
Count_0	31:0	ro	**Port 0 Receive Packet Count**

Other Port Registers have a similar structure as **RPC_0**; see **Table 22**.

Table 22 Port Registers RPC_x

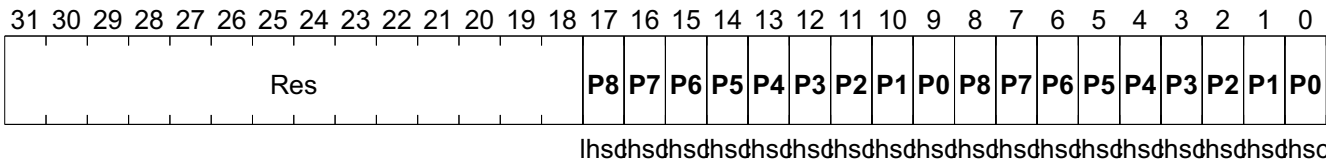
Register Short Name	Register Long Name	Offset Address	Page Number
RPC_1	Port 1 Receive Packet Count	05_H	
RPC_2	Port 2 Receive Packet Count	06_H	
RPC_3	Port 3 Receive Packet Count	07_H	
RPC_4	Port 4 Receive Packet Count	08_H	
RPC_5	Port 5 Receive Packet Count	09_H	
RPC_6	Port 6 Receive Packet Count	$0A_H$	
RPC_7	Port 7 Receive Packet Count	$0B_H$	
RPC_8	Port 8 Receive Packet Count	$0C_H$	
RPBC_0	Port 0 Receive Packet Byte Count	$0E_H$	
RPBC_1	Port 1 Receive Packet Byte Count	$0F_H$	
RPBC_2	Port 2 Receive Packet Byte Count	05_H	
RPBC_3	Port 3 Receive Packet Byte Count	10_H	
RPBC_4	Port 4 Receive Packet Byte Count	11_H	
RPBC_5	Port 5 Receive Packet Byte Count	12_H	
RPBC_6	Port 6 Receive Packet Byte Count	13_H	
RPBC_7	Port 7 Receive Packet Byte Count	14_H	
RPBC_8	Port 8 Receive Packet Byte Count	15_H	
TPC_0	Port 0 Transmit Packet Count	16_H	
TPC_1	Port 1 Transmit Packet Count	17_H	
TPC_2	Port 2 Transmit Packet Count	18_H	
TPC_3	Port 3 Transmit Packet Count	19_H	
TPC_4	Port 4 Transmit Packet Count	$1A_H$	
TPC_5	Port 5 Transmit Packet Count	$1B_H$	
TPC_6	Port 6 Transmit Packet Count	$1C_H$	
TPC_7	Port 7 Transmit Packet Count	$1D_H$	
TPC_8	Port 8 Transmit Packet Count	$1E_H$	
TPBC_0	Port 0 Transmit Packet Byte Count	$1F_H$	
TPBC_1	Port 1 Transmit Packet Byte Count	20_H	
TPBC_2	Port 2 Transmit Packet Byte Count	21_H	
TPBC_3	Port 3 Transmit Packet Byte Count	22_H	
TPBC_4	Port 4 Transmit Packet Byte Count	23_H	
TPBC_5	Port 5 Transmit Packet Byte Count	24_H	
TPBC_6	Port 6 Transmit Packet Byte Count	25_H	
TPBC_7	Port 7 Transmit Packet Byte Count	26_H	

Table 22 Port Registers RPC_x (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
TPBC_8	Port 8 Transmit Packet Byte Count	27_H	
CC_0	Port 0 Collision Count	28_H	
CC_1	Port 1 Collision Count	29_H	
CC_2	Port 2 Collision Count	$2A_H$	
CC_3	Port 3 Collision Count	$2B_H$	
CC_4	Port 4 Collision Count	$2C_H$	
CC_5	Port 5 Collision Count	$2D_H$	
CC_6	Port 6 Collision Count	$2E_H$	
CC_7	Port 7 Collision Count	$2F_H$	
CC_8	Port 8 Collision Count	30_H	
EC_0	Port 0 Error Count	31_H	
EC_1	Port 1 Error Count	32_H	
EC_2	Port 2 Error Count	33_H	
EC_3	Port 3 Error Count	34_H	
EC_4	Port 4 Error Count	35_H	
EC_5	Port 5 Error Count	36_H	
EC_6	Port 6 Error Count	37_H	
EC_7	Port 7 Error Count	38_H	
EC_8	Port 8 Error Count	39_H	

Over Flow Flag 0 Register

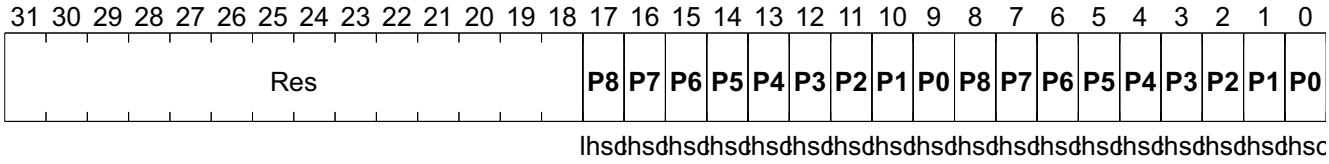
OFFR_0	Offset	Reset Value
Over Flow Flag 0 Register	$3A_H$	$0000\ 0000_H$



Field	Bits	Type	Description
P8	17	lhsc	**Overflow of Port 8 Receive Packet Byte Count**
P7	16	lhsc	**Overflow of Port 7 Receive Packet Byte Count**
P6	15	lhsc	**Overflow of Port 6 Receive Packet Byte Count**
P5	14	lhsc	**Overflow of Port 5 Receive Packet Byte Count**
P4	13	lhsc	**Overflow of Port 4 Receive Packet Byte Count**
P3	12	lhsc	**Overflow of Port 3 Receive Packet Byte Count**
P2	11	lhsc	**Overflow of Port 2 Receive Packet Byte Count**
P1	10	lhsc	**Overflow of Port 1 Receive Packet Byte Count**
P0	9	lhsc	**Overflow of Port 0 Receive Packet Byte Count**
P8	8	lhsc	**Overflow of Port 8 Receive Packet Count**
P7	7	lhsc	**Overflow of Port 7 Receive Packet Count**
P6	6	lhsc	**Overflow of Port 6 Receive Packet Count**
P5	5	lhsc	**Overflow of Port 5 Receive Packet Count**
P4	4	lhsc	**Overflow of Port 4 Receive Packet Count**
P3	3	lhsc	**Overflow of Port 3 Receive Packet Count**
P2	2	lhsc	**Overflow of Port 2 Receive Packet Count**
P1	1	lhsc	**Overflow of Port 1 Receive Packet Count**
P0	0	lhsc	**Overflow of Port 0 Receive Packet Count**

Over Flow Flag 1 Register

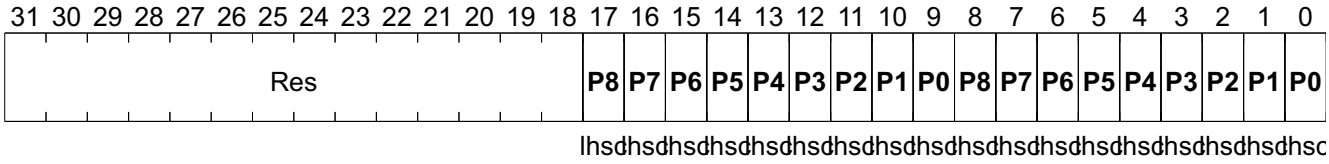
OFFR_1	Offset	Reset Value
Over Flow Flag 1 Register	$3B_H$	$0000\ 0000_H$



Field	Bits	Type	Description
P8	17	lhsc	**Overflow of Port 8 Transmit Packet Byte Count**
P7	16	lhsc	**Overflow of Port 7 Transmit Packet Byte Count**
P6	15	lhsc	**Overflow of Port 6 Transmit Packet Byte Count**
P5	14	lhsc	**Overflow of Port 5 Transmit Packet Byte Count**
P4	13	lhsc	**Overflow of Port 4 Transmit Packet Byte Count**
P3	12	lhsc	**Overflow of Port 3 Transmit Packet Byte Count**
P2	11	lhsc	**Overflow of Port 2 Transmit Packet Byte Count**
P1	10	lhsc	**Overflow of Port 1 Transmit Packet Byte Count**
P0	9	lhsc	**Overflow of Port 0 Transmit Packet Byte Count**
P8	8	lhsc	**Overflow of Port 8 Transmit Packet Count**
P7	7	lhsc	**Overflow of Port 7 Transmit Packet Count**
P6	6	lhsc	**Overflow of Port 6 Transmit Packet Count**
P5	5	lhsc	**Overflow of Port 5 Transmit Packet Count**
P4	4	lhsc	**Overflow of Port 4 Transmit Packet Count**
P3	3	lhsc	**Overflow of Port 3 Transmit Packet Count**
P2	2	lhsc	**Overflow of Port 2 Transmit Packet Count**
P1	1	lhsc	**Overflow of Port 1 Transmit Packet Count**
P0	0	lhsc	**Overflow of Port 0 Transmit Packet Count**

Over Flow Flag 2 Register

OFFR_2	Offset	Reset Value
Over Flow Flag 2 Register	$3C_H$	$0000\ 0000_H$



Field	Bits	Type	Description
P8	17	lhsc	**Overflow of Port 8 Error Count**
P7	16	lhsc	**Overflow of Port 7 Error Count**
P6	15	lhsc	**Overflow of Port 6 Error Count**
P5	14	lhsc	**Overflow of Port 5 Error Count**
P4	13	lhsc	**Overflow of Port 4 Error Count**
P3	12	lhsc	**Overflow of Port 3 Error Count**
P2	11	lhsc	**Overflow of Port 2 Error Count**
P1	10	lhsc	**Overflow of Port 1 Error Count**
P0	9	lhsc	**Overflow of Port 0 Error Count**
P8	8	lhsc	**Overflow of Port 8 Collision Count**
P7	7	lhsc	**Overflow of Port 7 Collision Count**
P6	6	lhsc	**Overflow of Port 6 Collision Count**
P5	5	lhsc	**Overflow of Port 5 Collision Count**
P4	4	lhsc	**Overflow of Port 4 Collision Count**
P3	3	lhsc	**Overflow of Port 3 Collision Count**
P2	2	lhsc	**Overflow of Port 2 Collision Count**
P1	1	lhsc	**Overflow of Port 1 Collision Count**
P0	0	lhsc	**Overflow of Port 0 Collision Count**

4.2 Serial Interface Timing

ADM6999G/GX serial chip internal counter or EEPROM access timing.

- EESK: Similar as MDC signal
- EDI: Similar as MDIO
- ECS: Must keep low

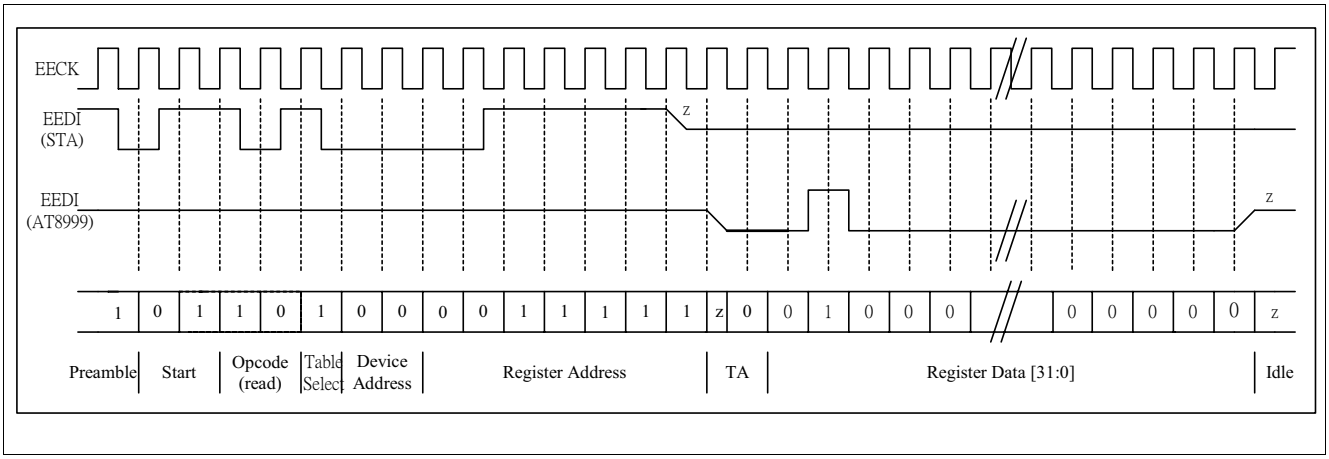


Figure 9 Serial Interface Timing X

- Preamble: At least 32 continuous "1".
- Start: 01(2 bits)
- Opcode: 10 (2 bits, Only supports read command)
- Table select: 1/Counter, 0/ EEPROM (1 bit)
- Register Address: Read Target register address. (7 bits)
- TA: Turn Around.
- Register Data: 32 bit data.
- Counter output bit sequence is bit 31 to bit 0.
- If users read EEPROM then 32 bits data will be separated in two EEPROM registers. The sequence is:
  - Register +1, Register (Register is even number).
  - Register, Register-1(Register is Odd number).
  - Example: Read Register 00_H then ADM6999G/GX will drive 01_H & 00_H.Read Register 03_H then ADM6999G/GX will drive 03_H & 02_H
- Idle: EESK must send at least one clock at idle time.

ADM6999G/GX issue Reset internal counter command

- EESK: Similar as MDC signal
- EDI: Similar as MDIO
- ECS: Must keep low

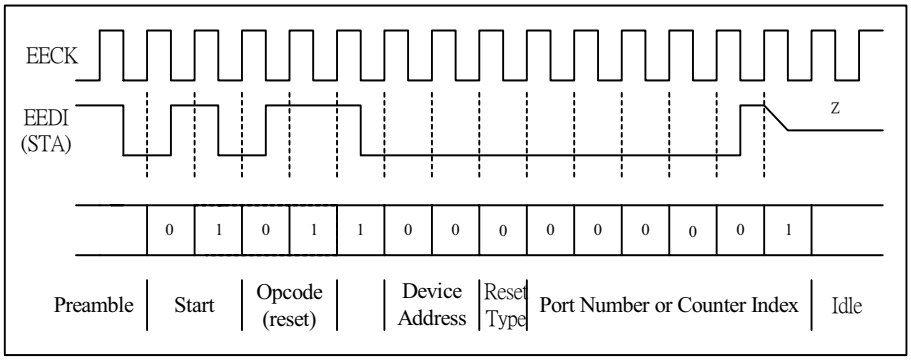


Figure 10 Serial Interface Timing Y

- Preamble: At least 32 continuous “1”
- Start: 01 (2 bits)
- Opcode: 01 (2 bits, Reset command)
- Device Address: Chip physical address as PHYAS[1:0]
- Reset_type: Reset counter by port number or by counter index
  - 1: Clear dedicate port’s all counters
  - 0: Clear dedicate counter
- Port_number or counter index: User define clear port or counter
- Idle: EECK must send at least one clock at idle time

5 ADM6999GTX/FX Interface

5.1 TP Interface

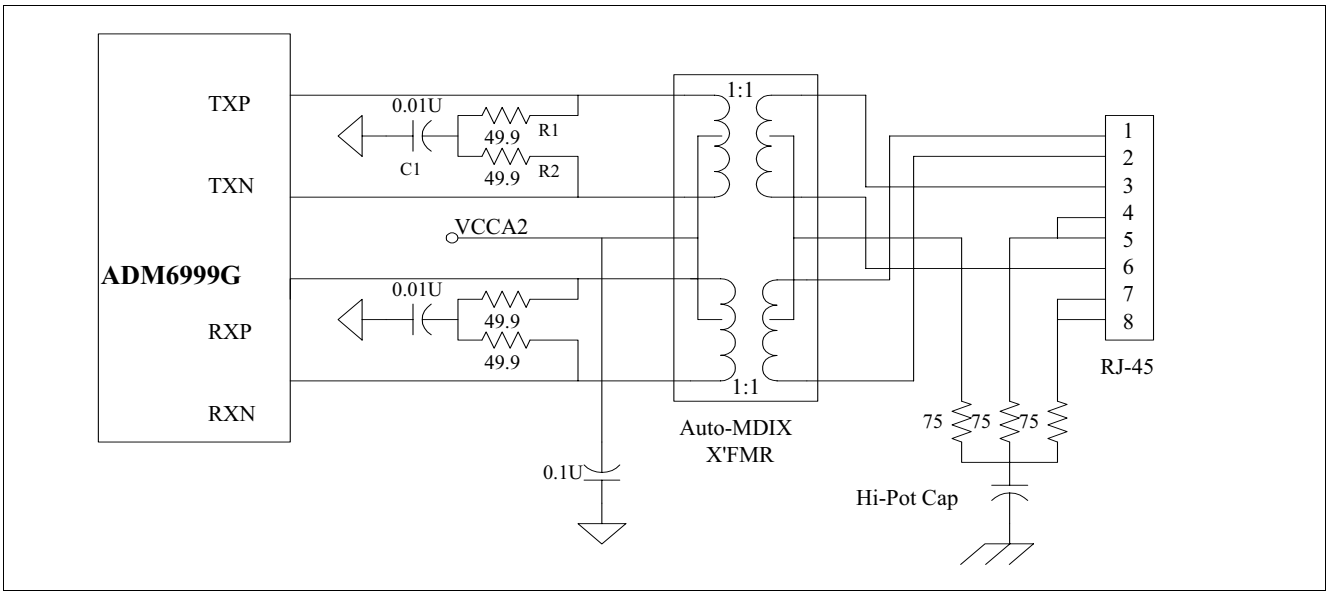


Figure 11 TP Interface

Transformer requirements:

- TX/RX rate 1:1
- TX/RX central tap connect together to VCCA2.

Users can change TX/RX pin for easy layout but do not change polarity. ADM6999G/GX supports auto polarity on receiving side.

5.2 FX Interface

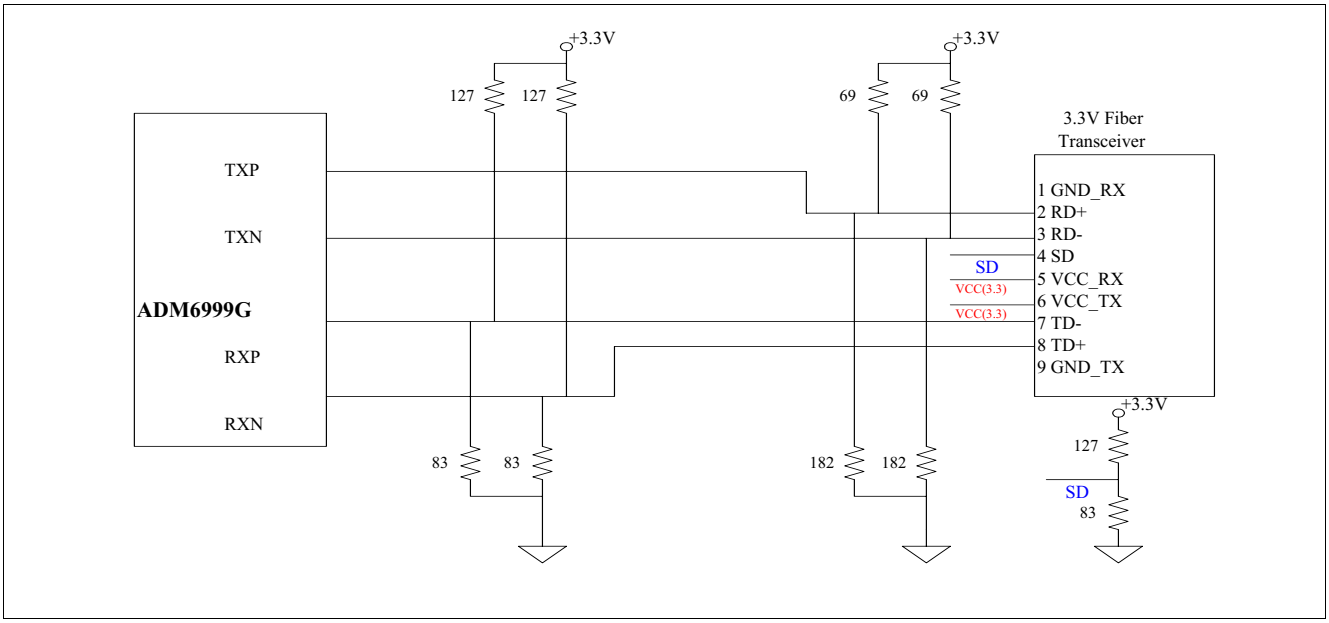


Figure 12 FX Interface

6 DC Characteristics

Table 23 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Supply	V_{CC}	-0.3	–	3.63	V	–
TX line driver	V_{cca2}	–	–	1.8	V	–
PLL voltage	V_{ccpll}	–	–	1.8	V	–
Digital core voltage	V_{ccik}	–	–	1.8	V	–
Input Voltage	V_{IN}	-0.3	–	V_{CC} + 0.3	V	–
Output Voltage	V_{out}	-0.3	–	V_{CC} + 0.3	V	–
Storage Temperature	T_{STG}	-55	–	155	°C	–
Power Dissipation	PD	–	–	1.8	W	–
ESD Rating	ESD	–	–	2	KV	–

Table 24 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Supply	V_{CC}	2.8	3.3	3.465	V	–
TX line driver	V_{cca2}	1.7	1.8	1.9	V	–
PLL voltage	V_{ccpll}	1.7	1.8	1.9	V	–
Digital core voltage	V_{ccik}	1.7	1.8	1.9	V	–
Input Voltage	V_{in}	0	–	V_{CC}	V	–
Power consumption	PC	–	1.8	–	W	–
Junction Operating Temperature	T_j	0	25	115	°C	–

Table 25 DC Electrical Characteristics for 3.3 V Operation[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Low Voltage	V_{IL}	–	–	0.3 * V_{CC}	V	CMOS
Input High Voltage	V_{IH}	0.7 * V_{CC}	–	–	V	CMOS
Output Low Voltage	V_{OL}	–	–	0.4	V	CMOS
Output High Voltage	V_{OH}	0.7 * V_{CC}	–	–	V	CMOS
Input Pull-up/down Resistance	R_I	–	100	–	kΩ	V_{IL} = 0 V or V_{IH} = V_{CC}

1) (under V_{CC} = 3.0 V ~ 3.6 V, T_j = 0 °C ~ 115 °C)

7 AC Characteristics

7.1 Power On Reset

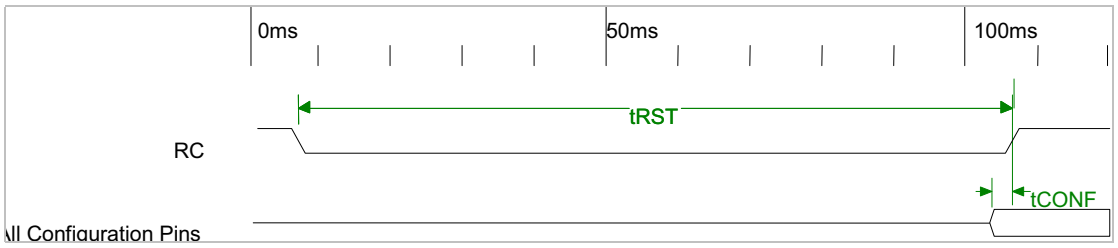


Figure 13 Power On Reset

Table 26 Power On Reset

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RST Low Period	T_{RST}	100	–	–	ms	–
Start of Idle Pulse Width	T_{CONF}	100	–	–	ns	–

7.2 EEPROM Data Timing

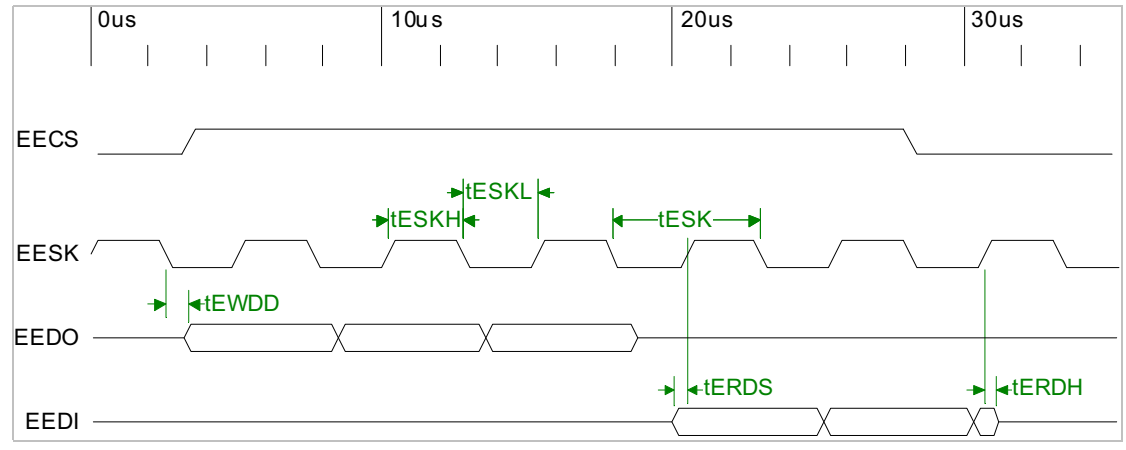


Figure 14 EEPROM Data Timing

Table 27 EEPROM Data Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EESK Period	T_{ESK}	–	5120	–	ns	–
EESK Low Period	T_{ESKL}	2550	–	2570	ns	–
EESK High Period	T_{ESKH}	2550	–	2570	ns	–
EEDI to EESK Rising Setup Time	T_{ERDS}	10	–	–	ns	–
EEDI to EESK Rising Hold Time	T_{ERDH}	10	–	–	ns	–
EESK Falling to EEDO Output Delay Time	T_{EWDD}	–	–	20	ns	–

7.3 10Base-TX MII Input Timing

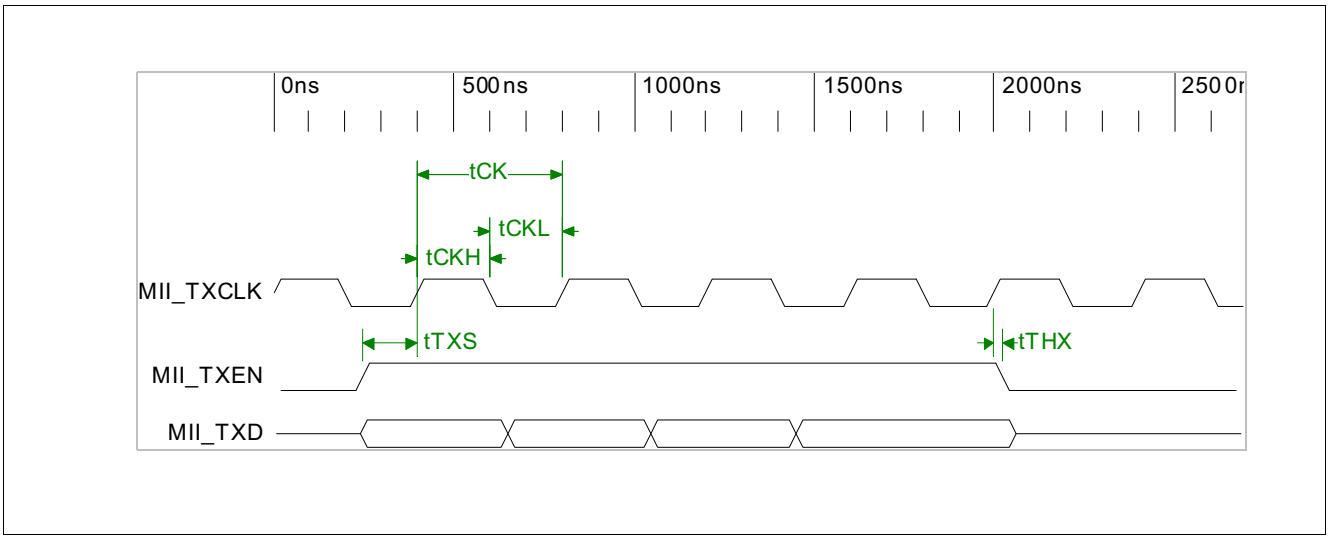


Figure 15 10Base-TX MII Input Timing

Table 28 10Base-TX MII Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_TXCLK Period	T_{CK}	–	400	–	ns	–
MII_TXCLK Low Period	T_{CKL}	160	–	240	ns	–
MII_TXCLK High Period	T_{CKH}	160	–	240	ns	–

Table 28 10Base-TX MII Input Timing (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_TXD, MII_TXEN to MII_TXCLK Rising Setup Time	T_{TXS}	10	–	–	ns	–
MII_TXD, MII_TXEN to MII_TXCLK Rising Hold Time	T_{TXH}	10	–	–	ns	–

7.4 10Base-TX MII Output Timing

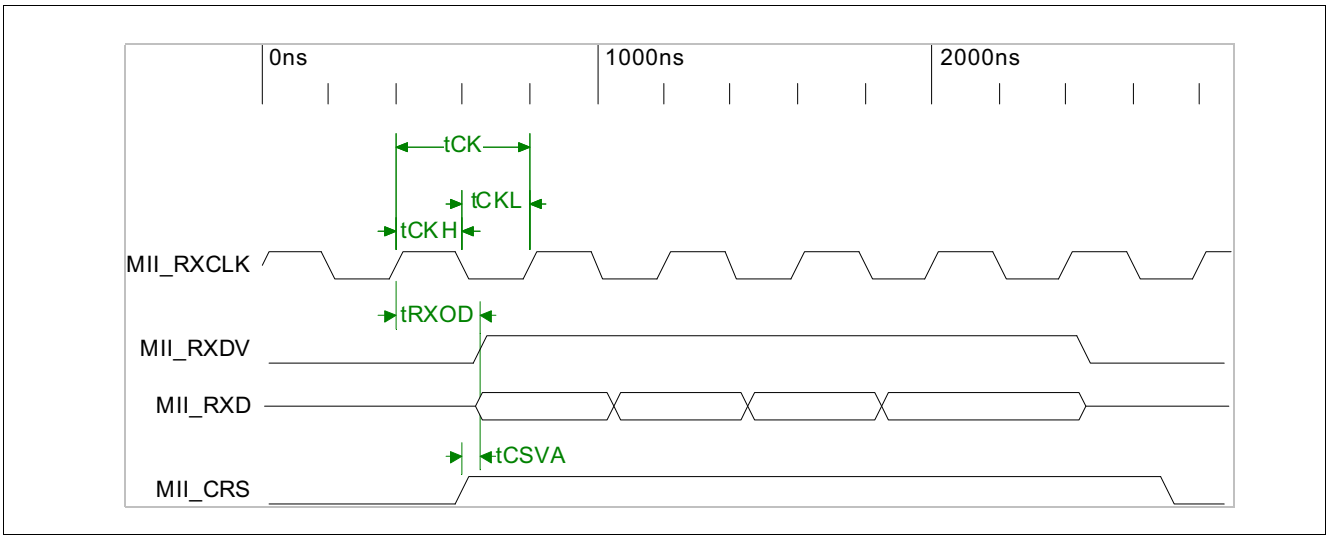


Figure 16 10Base-TX MII Output Timing

Table 29 10Base-TX MII Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_RXCLK Period	T_{CK}	–	400	–	ns	–
MII_RXCLK Low Period	T_{CKL}	160	–	240	ns	–
MII_RXCLK High Period	T_{CKH}	160	–	240	ns	–
MII_CRS Rising to MII_RXDV Rising	T_{CSVA}	0	–	10	ns	–
MII_RXCLK Rising to MII_RXD, MII_RXDV, MII_CRS Output Delay	T_{RXOD}	200	–	–	ns	–

7.5 100Base-TX MII Input Timing

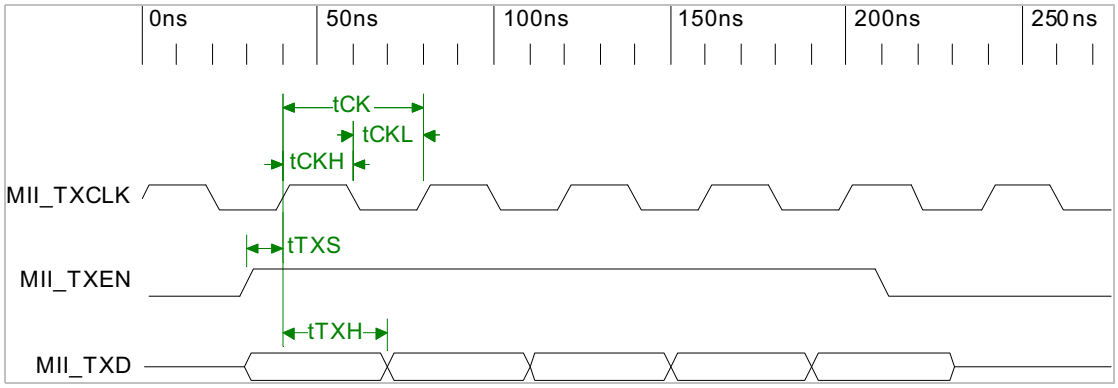


Figure 17 100Base-TX MII Input Timing

Table 30 100Base-TX MII Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_TXCLK Period	T_{CK}	–	40	–	ns	–
MII_TXCLK Low Period	T_{CKL}	16	–	24	ns	–
MII_TXCLK High Period	T_{CKH}	16	–	24	ns	–
MII_TXD, MII_TXEN to MII_TXCLK Rising Setup Time	T_{TXS}	10	–	–	ns	–
MII_TXD, MII_TXEN to MII_TXCLK Rising Hold Time	T_{TXH}	10	–	–	ns	–

7.6 100Base-TX MII Output Timing

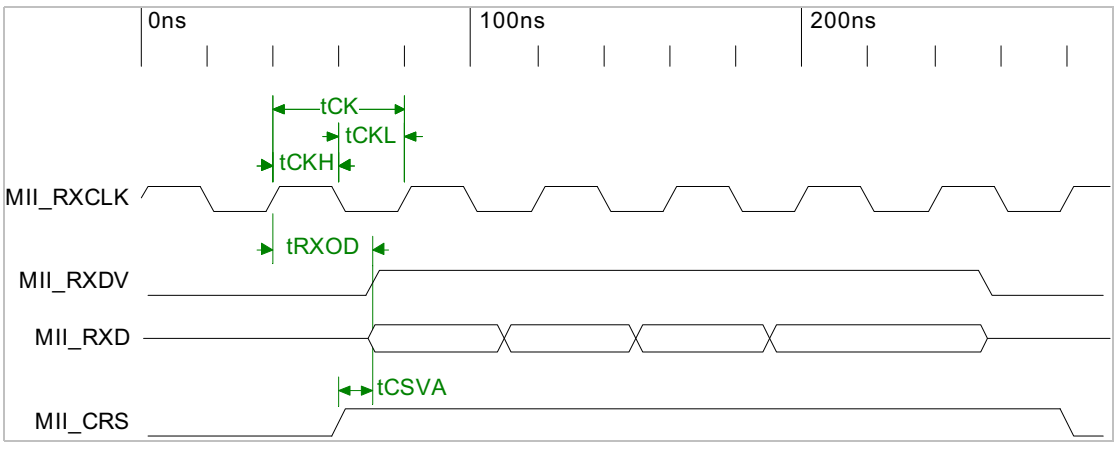


Figure 18 100Base-TX MII Output Timing

Table 31 100Base-TX MII Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_RXCLK Period	T_{CK}	–	40	–	ns	–
MII_RXCLK Low Period	T_{CKL}	16	–	24	ns	–
MII_RXCLK High Period	T_{CKH}	16	–	24	ns	–
MII_CRS Rising to MII_RXDV Rising	T_{CSVA}	0	–	10	ns	–
MII_RXCLK Rising to MII_RXD, MII_RXDV, MII_CRS Output Delay	T_{RXOD}	20	–	30	ns	–

7.7 GMII Receive Signals Timing

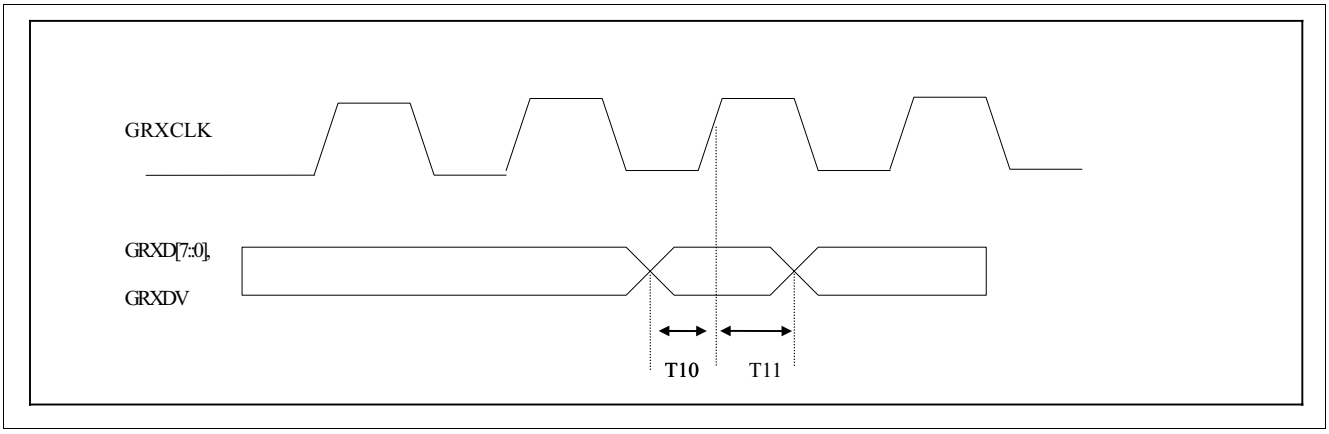


Figure 19 GMII Receive Signals Timing

Table 32 GMII Receive Signals Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Setup Time to Rising GRXCLK	T_{10}	2	–	–	ns	–
Hold Time to Rising GRXCLK	T_{11}	0.5	–	–	ns	–

7.8 GMII Transmit Signals Timing

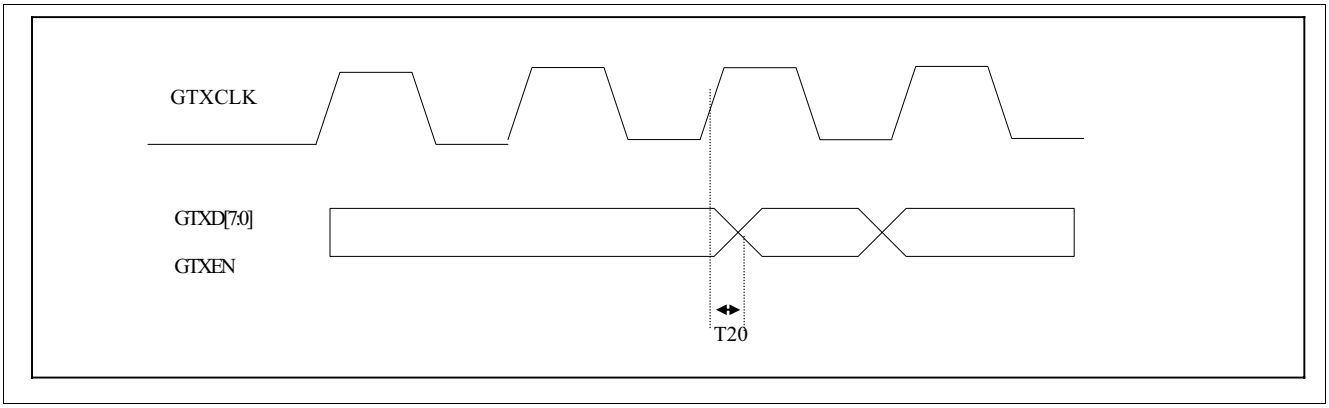


Figure 20 GMII Transmit Signals Timing

Table 33 GMII Transmit Signals Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data Valid Delay after Rising GTXCLK	T_{20}	1.5	–	4	ns	–

7.9 SMI Timing

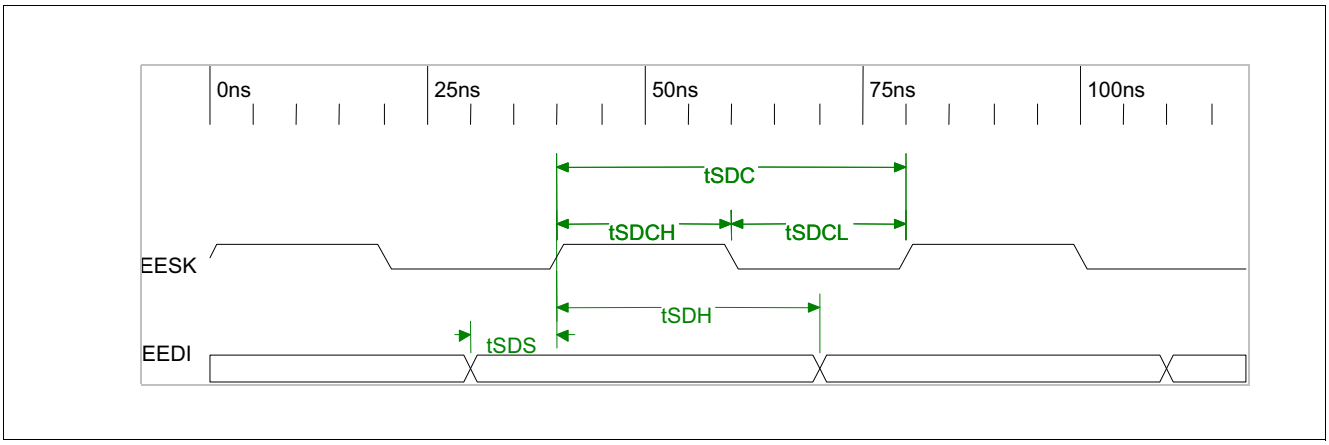


Figure 21 SMI Timing

Table 34 SMI Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EESK Period	T_{CK}	20	–	–	ns	–
EESK Low Period	T_{CKL}	10	–	–	ns	–
EESK High Period	T_{CKH}	10	–	–	ns	–
EEDI to EESK rising setup time on read/write cycle	T_{SDS}	4	–	–	ns	–
EEDI to EESK rising hold time on read/write cycle	T_{SDH}	2	–	–	ns	–

8 Package

ADM6999G/GX 128 Pin PQFP Outside Dimension

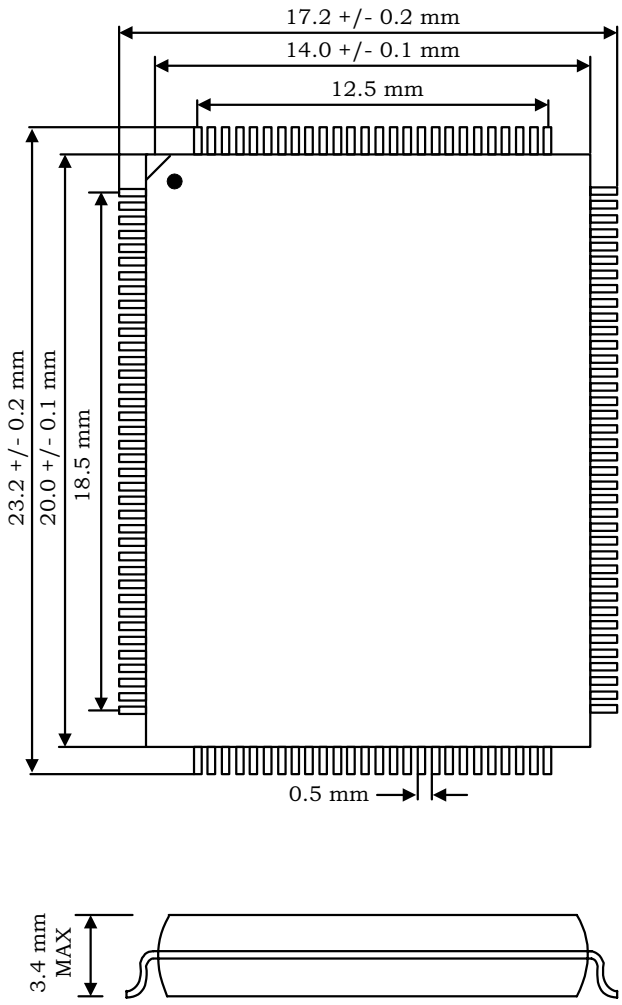


Figure 22 ADM6999G/GX 128 Pin PQFP Outside Dimension

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